

CONTENT	SHEET
Cover Sheet, Block Diagram	1-2
Intel LGA1366 CPU	3-8
DDR3 Chanel-A / Chanel-B / Chanel-C	9-11
Intel IOH 36S	12-19
ICH10R	20-22
Clock Gen ICS9LPRS113	23
PCI SLOT1	24
PCI-E X16 SLOT1 , 2 , 3	25
PCI-E SW / X1 SLOT	26
SIO-Fintek F71882F	27
LAN1 / LAN2 - BCM5784M	28-29
Audio Codec ALC888S	30
1394 Controller - TI TSB43AB22A	31
JMB-363 ODD_SATA / IDE	32
SIL3132 - eSATA	33
USB Connector	34
VRD11.1 - ISL6336 6-Phase	35
CPU_VTT - ISL6314 1-Phase	36
ACPI Controller UPI	37
NB Core Power & DDR Power	38
ATX Connector/F_Panel	39
ICH SATA / FAN Control	40
EMI	41
XDP PORT/ Manual Parts	42-43
GPIO Setting / PCI Routing / Power Map	44-45
Reset & PWROK Map / 6-layer PCB Stack-up	46-47
Revision History	48

# MS-7543 ATX Version: 0C

**CPU:** BloomField Processors In LGA1366 Package.

## System Chipset:

Intel Tylersburg I/O Hub 36S (North Bridge)  
Intel ICH10R (South Bridge)

## On Board Devices:

CLOCK Gen -- ICS 9LPRS113  
LPC Super I/O -- Fintek F71882F  
Dual LAN --BCM5784M  
HD Audio Codec -- ALC888S  
1394 Controller -- TI TSB43AB22A  
ODD\_SATA /IDE -- JMB363  
eSATA -- SIL3123

## Main Memory:


3-Channel A / B / C DDR-III \*3

## Expansion Slots:

PCI EXPRESS X16 SLOT \*3  
PCI EXPRESS X1 SLOT \* 2  
PCI SLOT \* 1

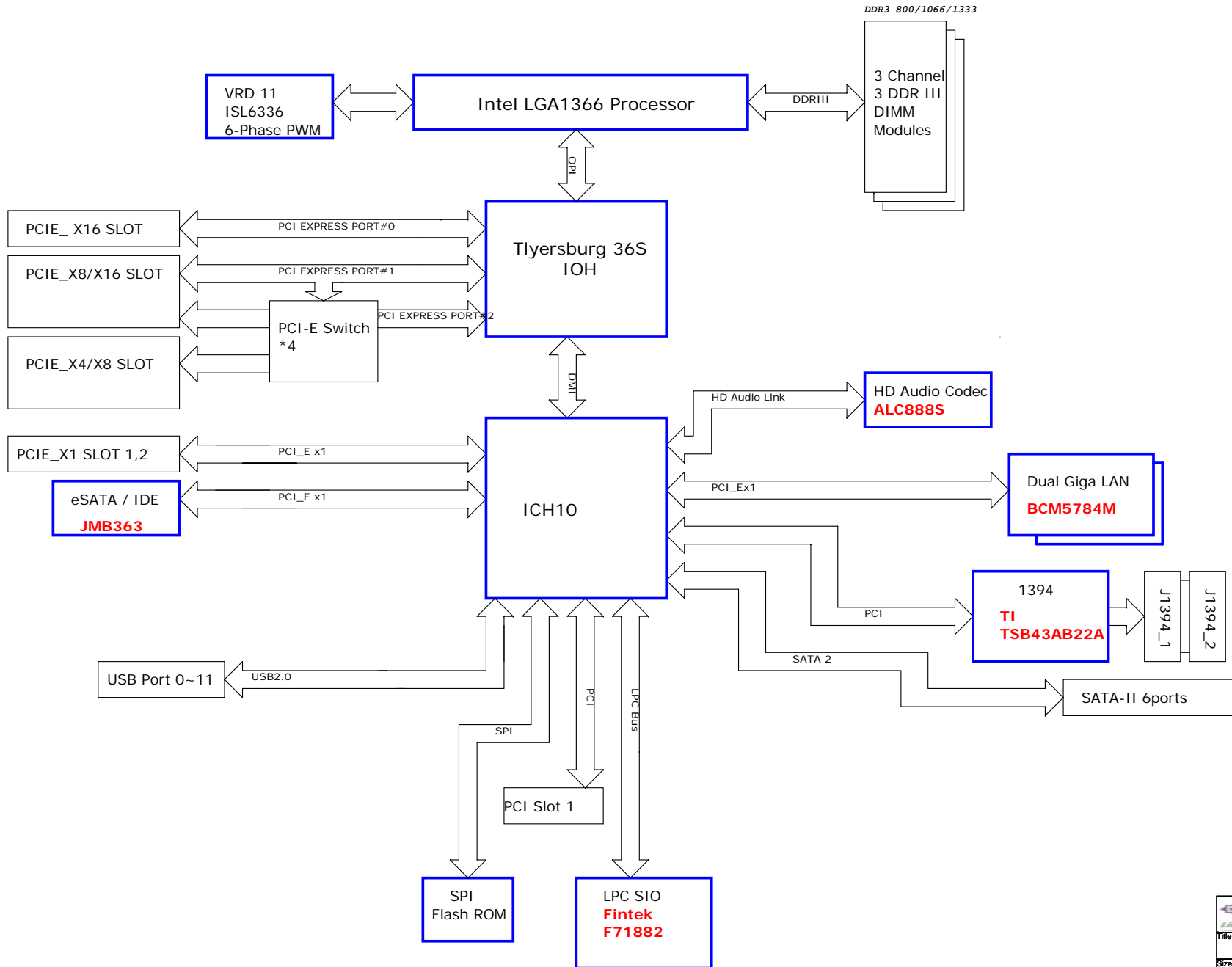
**PWM:** VR11.1 Intersil ISL6336 (6 Phases)

# DELL Suzuka MLK

 <b>MICRO-START INT'L CO.,LTD.</b>		
Title <b>COVER SHEET</b>		
Size	Document Number	Rev
Custom	<b>DELL Suzuka MLK (MS-7543)</b>	<b>0C</b>
Date:	Tuesday, September 09, 2008	Sheet 1 of 48



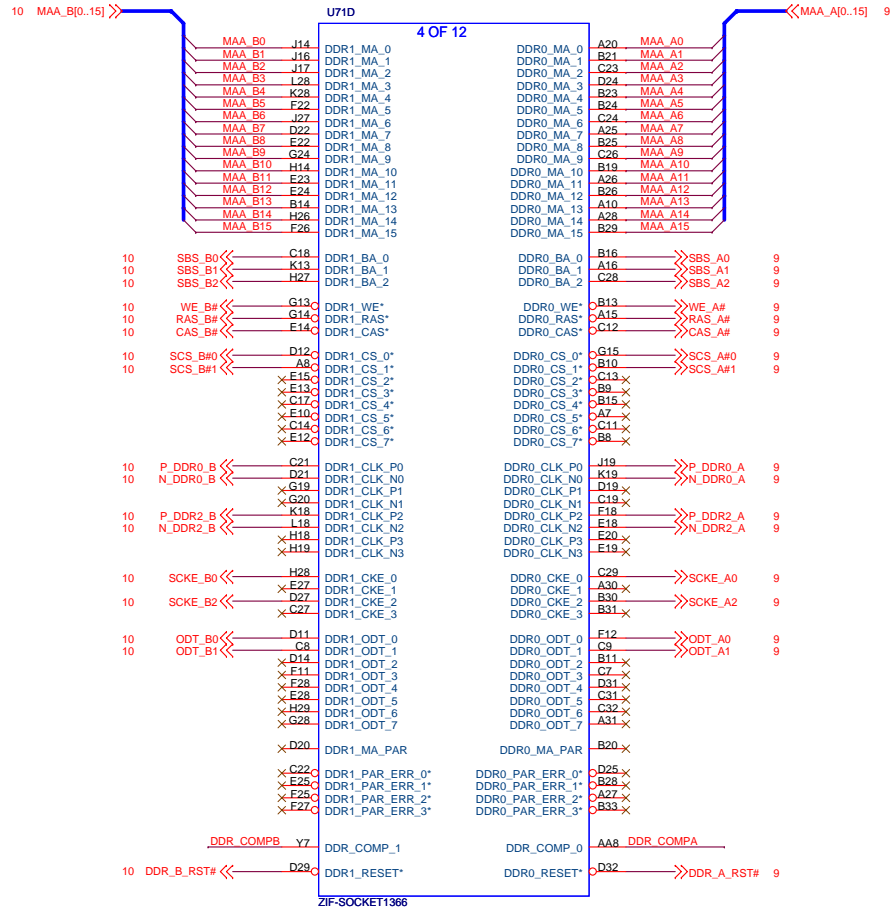
# Block Diagram



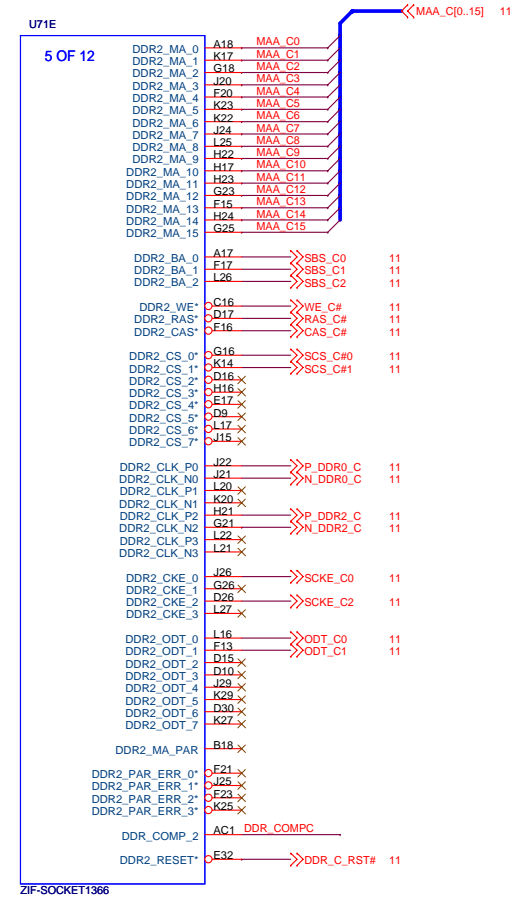
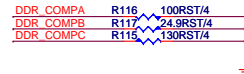








ZIF-SOCKET1366

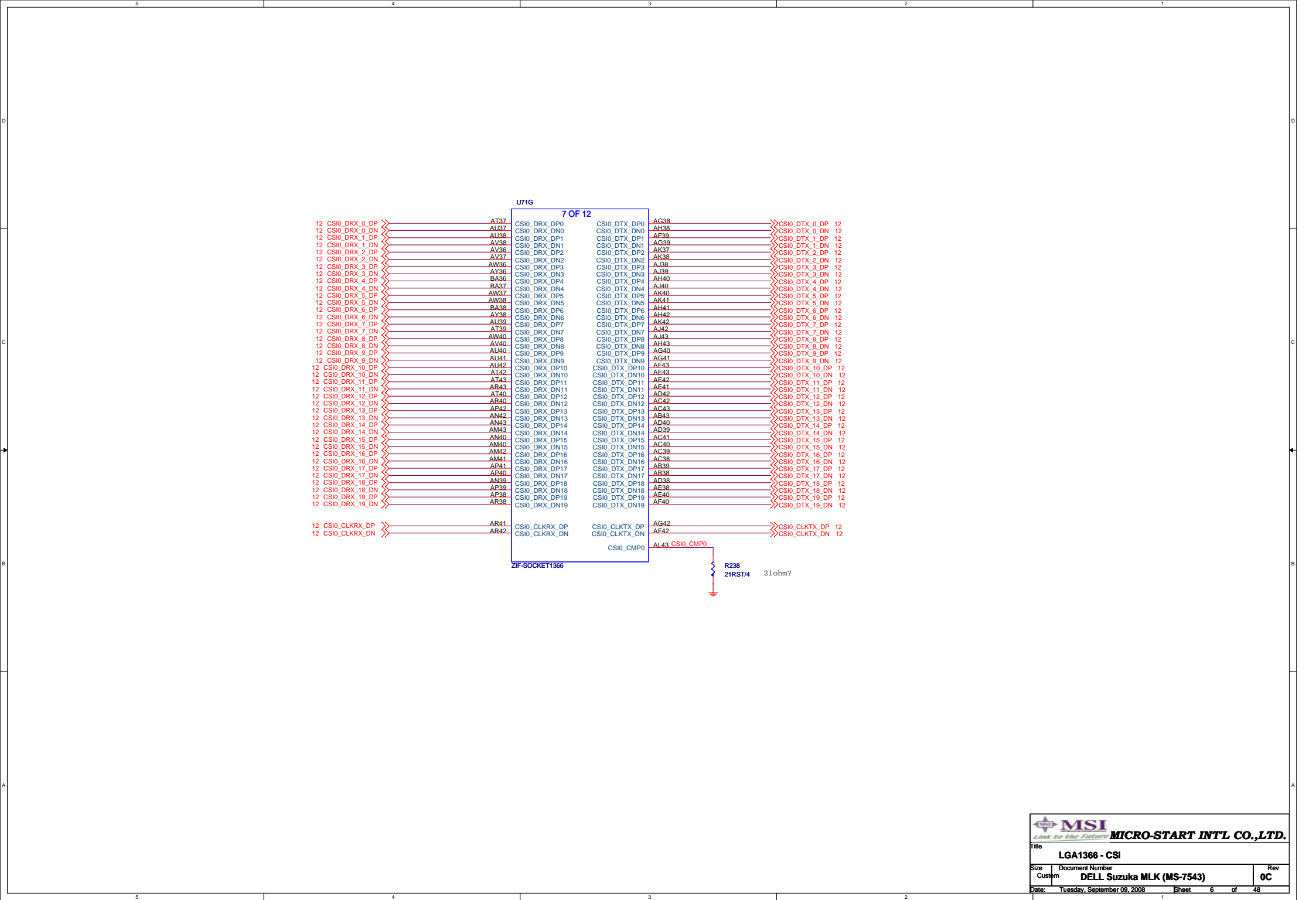


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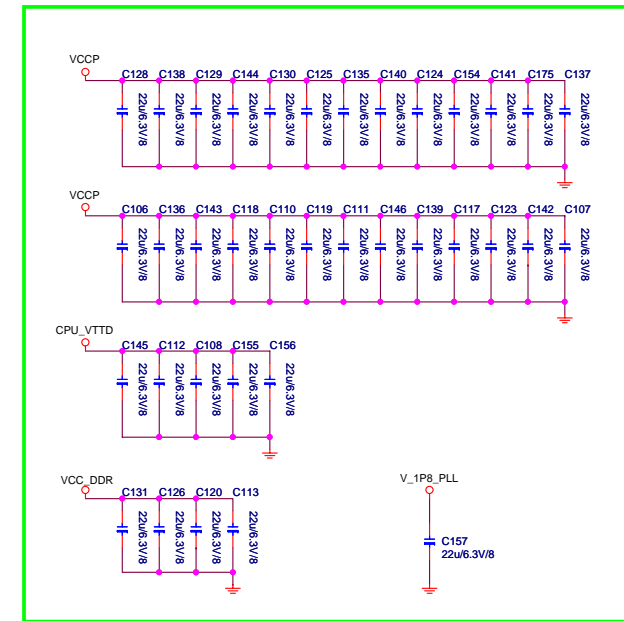
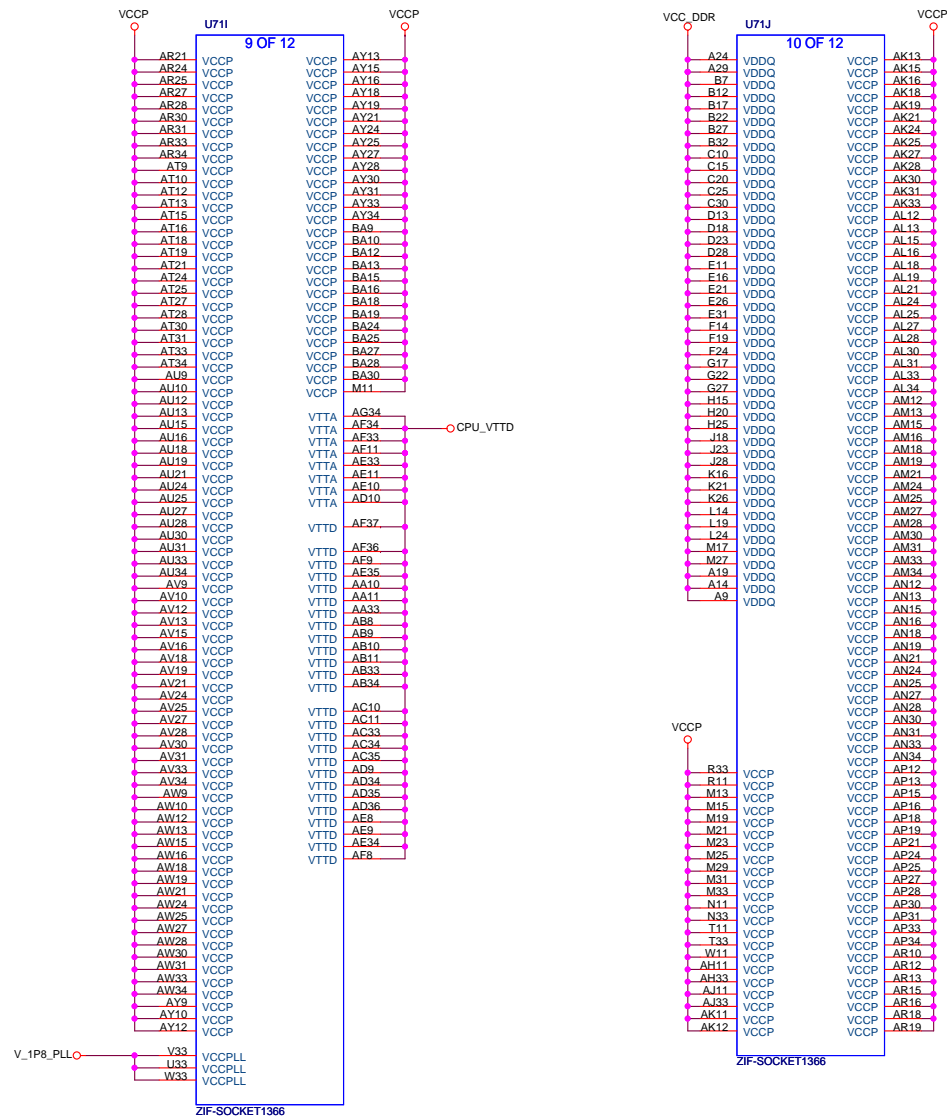












INSIDE CPU SOCKET



U71K		
11 OF 12		
B42	VSS	AV23
B37	VSS	AV22
B2	VSS	AV20
A41	VSS	AV17
A39	VSS	AV14
A35	VSS	AV11
A6	VSS	AV4
A4	VSS	AU43
C5	VSS	AU36
F6	VSS	AU22
E1	VSS	AU32
D43	VSS	AU29
D38	VSS	AU26
D33	VSS	AU23
D8	VSS	AU22
D3	VSS	AU20
C43	VSS	AU17
C40	VSS	AU14
C35	VSS	AU11
E36	VSS	AU5
F41	VSS	AU1
F4	VSS	AT41
F9	VSS	AT38
F29	VSS	AT35
F34	VSS	AT32
F39	VSS	AT29
G2	VSS	AT26
G7	VSS	AT23
G12	VSS	AT22
G32	VSS	AT20
G37	VSS	AT17
G42	VSS	AT14
H5	VSS	AT11
H10	VSS	AT8
H30	VSS	AT7
H35	VSS	AR39
BA39	VSS	AR35
BA35	VSS	AR32
BA29	VSS	AR29
BA26	VSS	AR26
BA20	VSS	AR23
BA17	VSS	AR22
BA14	VSS	AR20
BA11	VSS	AR17
BA5	VSS	AR14
BA3	VSS	AR11
AY42	VSS	AR3
AY37	VSS	AP36
AY32	VSS	AP33
AY29	VSS	AP37
AY26	VSS	AP36
AY23	VSS	AP35
AY22	VSS	AP32
AY20	VSS	AP29
AY17	VSS	AP26
AY14	VSS	AP23
AY11	VSS	AP22
AY7	VSS	AP17
AW35	VSS	AP14
AW32	VSS	AP11
AW29	VSS	AP10
AW26	VSS	AP6
AW23	VSS	AP5
AW22	VSS	AP1
AW20	VSS	AN41
AW17	VSS	AN37
AW14	VSS	AN35
AW11	VSS	AN32
AW8	VSS	AN29
AW6	VSS	AN26
AW1	VSS	AN23
AV41	VSS	AN22
AV39	VSS	AN20
AV32	VSS	AN17
AV29	VSS	AN14
AV26	VSS	AN11
	VSS	

ZIF-SOCKET1366

U71L		
12 OF 12		
AN7	VSS	AB40
AN3	VSS	AB37
AM39	VSS	AB7
AM37	VSS	AB4
AM35	VSS	AA39
AM32	VSS	AA38
AM29	VSS	AA34
AM26	VSS	AA9
AM23	VSS	AA3
AM22	VSS	Y41
AM20	VSS	Y36
AM17	VSS	Y33
AM14	VSS	Y11
AM11	VSS	Y6
AM9	VSS	Y1
AM5	VSS	W43
AL42	VSS	W38
AL37	VSS	W8
AL36	VSS	W3
AL35	VSS	V40
AL32	VSS	V35
AL29	VSS	V10
AL26	VSS	V5
AL23	VSS	U42
AL22	VSS	U37
AL20	VSS	U7
AL17	VSS	U2
AL14	VSS	T39
AL11	VSS	T34
AL7	VSS	T9
AL2	VSS	T4
AL1	VSS	R41
AK3	VSS	R36
AK39	VSS	R6
AK34	VSS	R1
AK32	VSS	P43
AK29	VSS	P38
AK26	VSS	P33
AK23	VSS	P11
AK22	VSS	P8
AK20	VSS	P3
AK17	VSS	N40
AK14	VSS	N35
AK10	VSS	N10
AK9	VSS	N6
AK3	VSS	M42
AJ41	VSS	M37
AJ36	VSS	M32
AJ34	VSS	M30
AJ5	VSS	M28
AH39	VSS	M26
AH37	VSS	M24
AH34	VSS	M22
AH7	VSS	M20
AH1	VSS	M18
AG43	VSS	M16
AG33	VSS	M14
AG11	VSS	M12
AG9	VSS	M7
AG3	VSS	M2
AF41	VSS	L39
AF38	VSS	L34
AF35	VSS	L29
AF5	VSS	L9
AE39	VSS	L4
AE7	VSS	K41
AE2	VSS	K36
AD43	VSS	K31
AD41	VSS	K11
AD33	VSS	K6
AD11	VSS	K1
AD37	VSS	J43
AC36	VSS	J38
AC9	VSS	J33
AC5	VSS	J13
AC2	VSS	J8
AB42	VSS	J3
AC7	VSS	H40

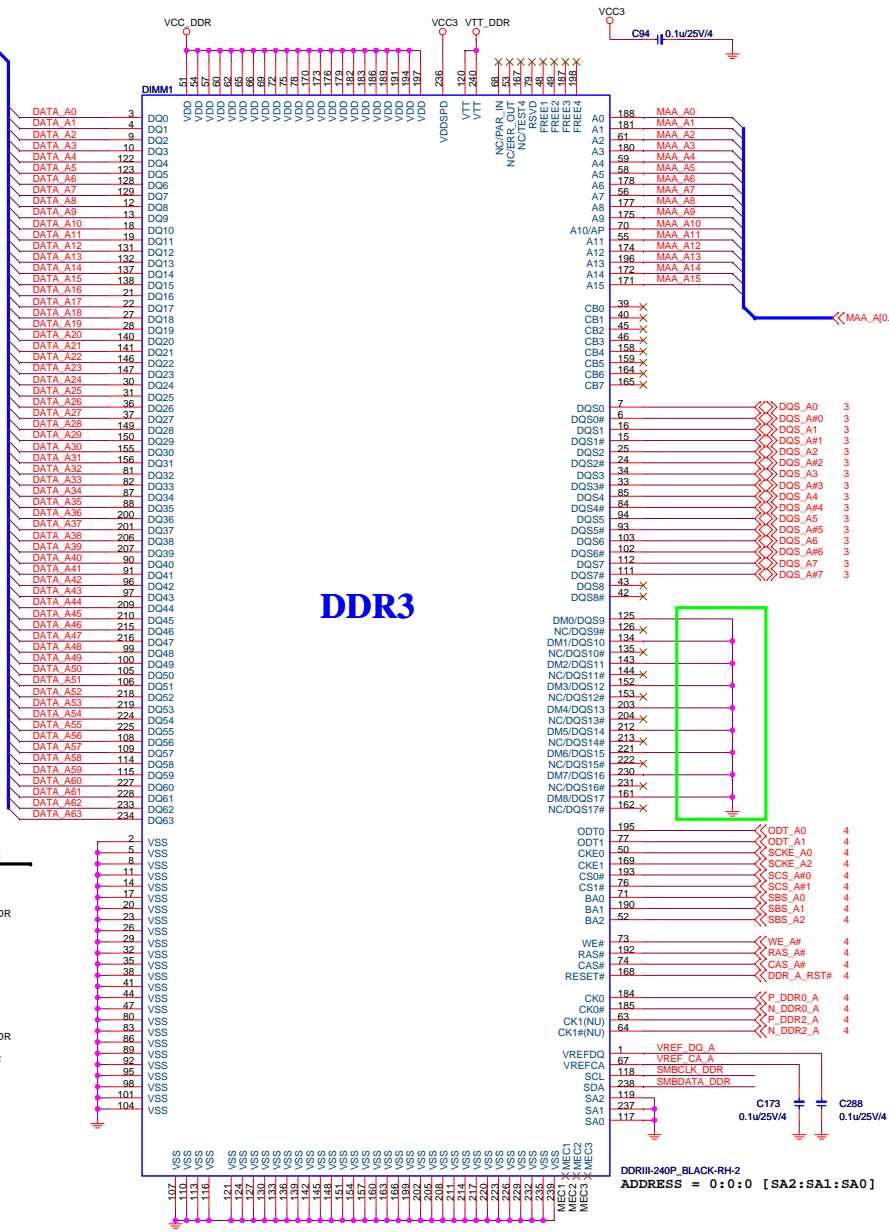
ZIF-SOCKET1366

U71H		
8 OF 12		
AM8	RSVD	AC8
AL8	RSVD	AD8
AM6	RSVD	AD5
AM7	RSVD	AD5
AN5	RSVD	AD6
AN6	RSVD	AD7
AM4	RSVD	AD6
AN4	RSVD	AC6
AP4	RSVD	AC4
AP4	RSVD	AD4
AM2	RSVD	AE3
AM3	RSVD	AE4
AN1	RSVD	AC3
AM1	RSVD	AB3
AP2	RSVD	AD2
AN2	RSVD	AD3
AR4	RSVD	AE1
AR5	RSVD	AD1
AT1	RSVD	AF2
AR1	RSVD	AF3
AT3	RSVD	AH2
AT2	RSVD	AC2
AL4	RSVD	AH3
AU3	RSVD	AH4
AW4	RSVD	AK1
AW3	RSVD	AJ1
AU7	RSVD	AJ3
AU6	RSVD	AJ2
AY6	RSVD	AG7
AY5	RSVD	AG6
BA7	RSVD	AJ4
BA6	RSVD	AK4
AV5	RSVD	AK6
AW5	RSVD	AK5
AB8	RSVD	AJ6
AV7	RSVD	AJ8
AW7	RSVD	AJ7
AU8	RSVD	AG8
AV8	RSVD	AH8
AT6	RSVD	
AR6	RSVD	
AE6	RSVD	
AE6	RSVD	AL6

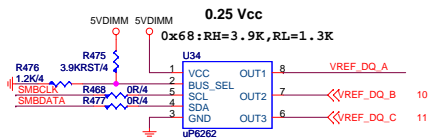
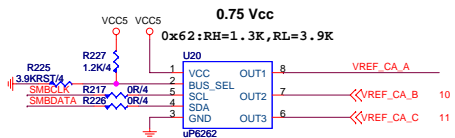
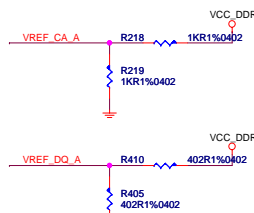
ZIF-SOCKET1366




## DIMM1 / CHANNEL A0



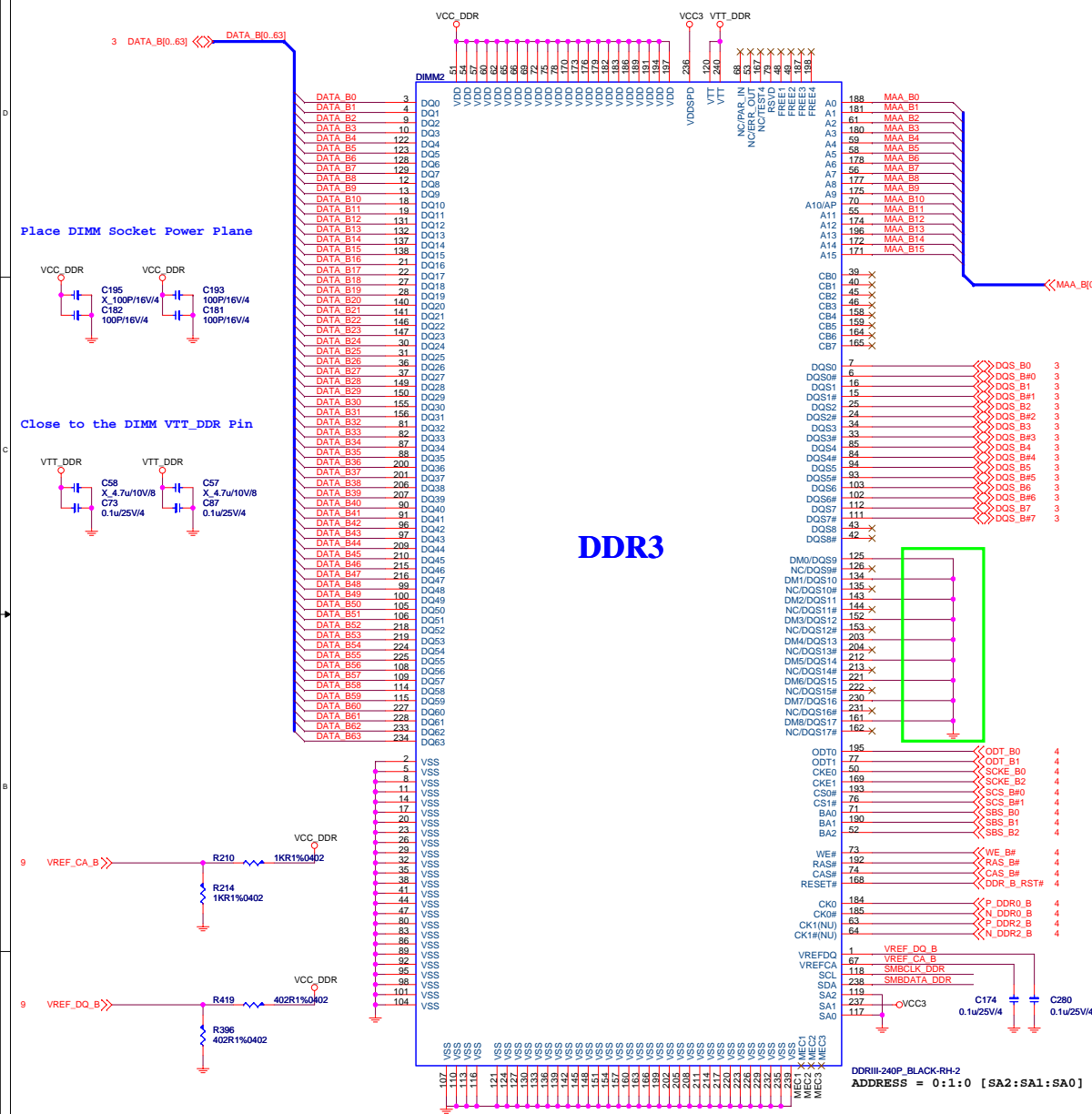
## UPI VOLTAGE CONSOLE



 <b>MSI</b> <i>Look to the Future</i>				<b>MICRO-START INT'L CO.,LTD.</b>			
<b>Title</b> <b>DDR III DIMM1</b>							
<b>Size</b> Custom		<b>Document Number</b> <b>DELL Suzuki MLK (MS-7543)</b>				<b>Rev</b> <b>0C</b>	
<b>Date:</b> Tuesday, September 09, 2008				<b>Sheet</b> 9		<b>of</b> 48	



# DIMM2 / CHANNEL B0



Vref-DQ : Reference voltage for DQ0-DQ63, CB0-CB7 and PAR\_IN. When in single ended mode used for DQS0-DQS7.

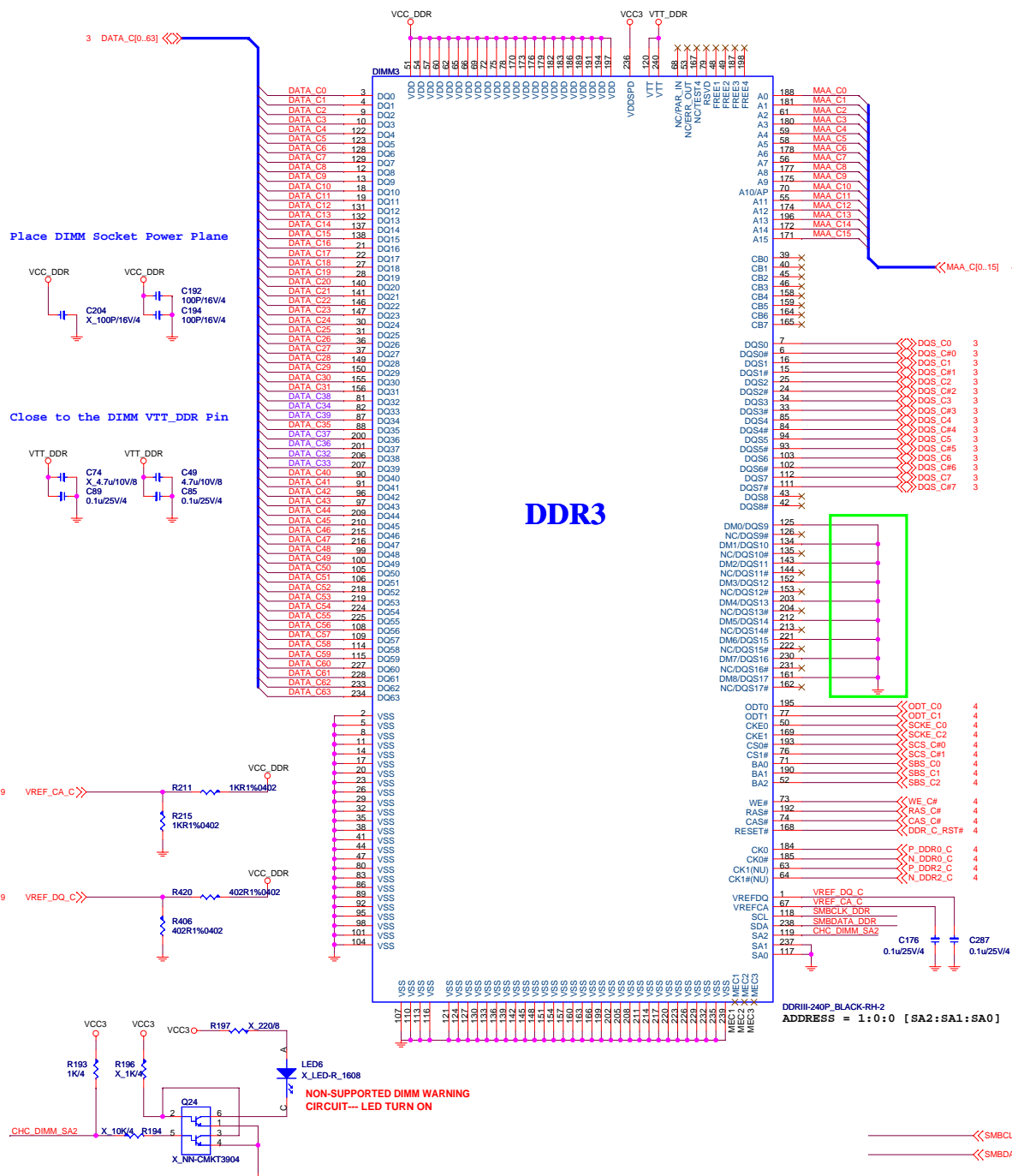
Vref-CA : Reference voltage for A0-A15, BA0-BA2, RAS#, CAS#, WE#, S0#, S01#, CKE0, CKE1, ODT0 and ODT1.

RESET#(Output) : A synchronously forces all registered output LOW when RESET# is LOW. This signal can be used during power up to ensure that CKE is LOW and DQs are High-Z.

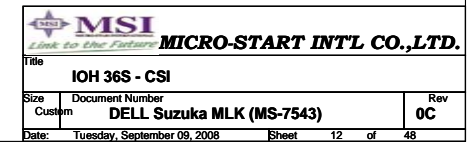
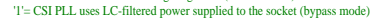
SMCLK\_DDR 9,11  
SMBDATA\_DDR 9,11



### DIMM3 / CHANNEL C0



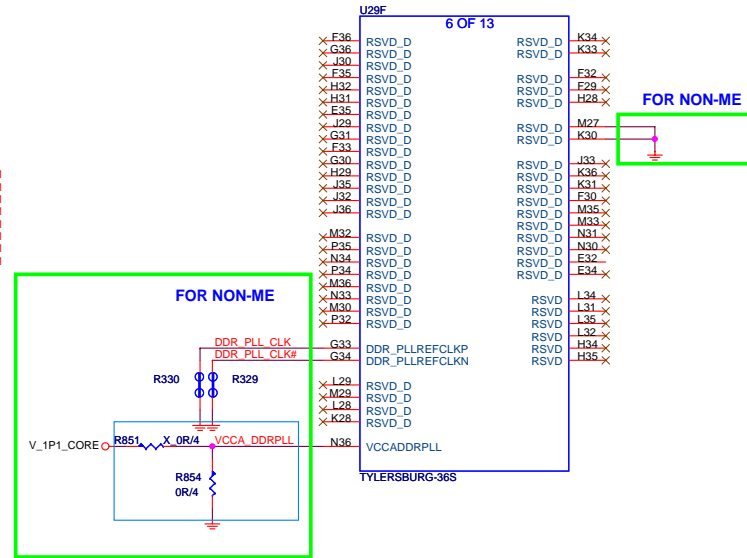
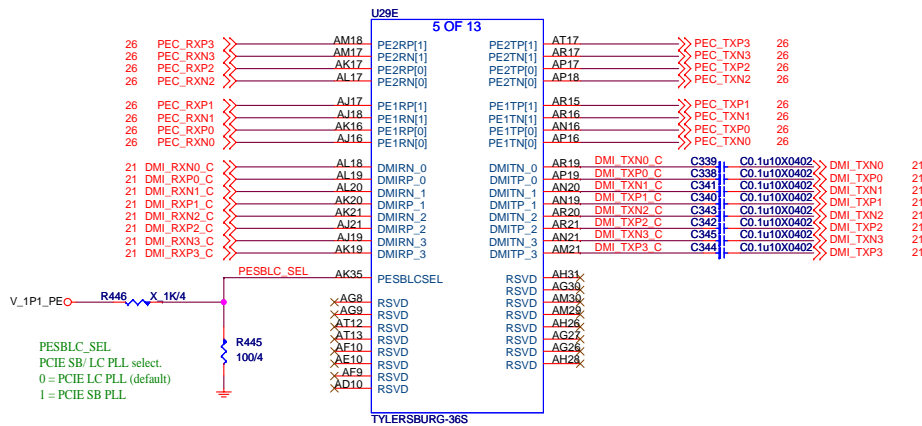




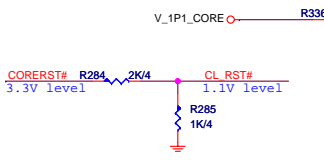
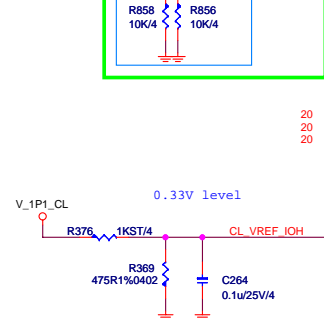
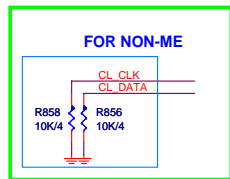






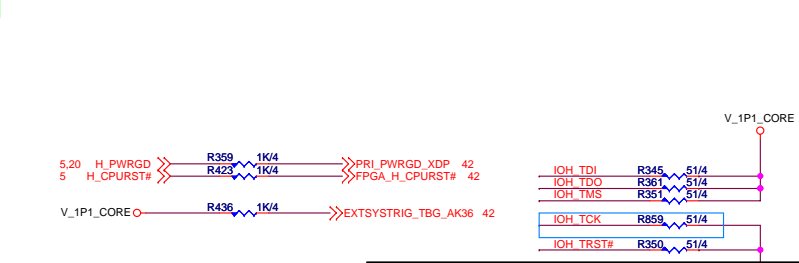
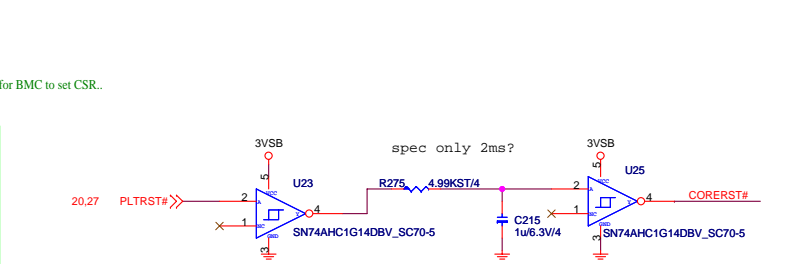
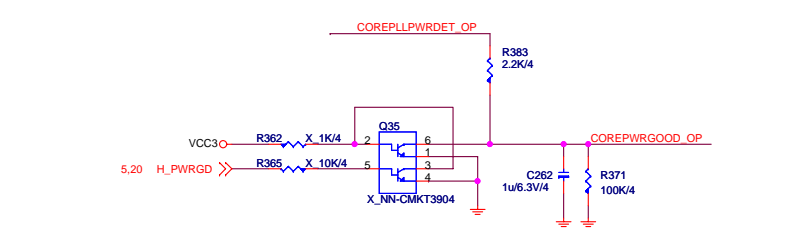
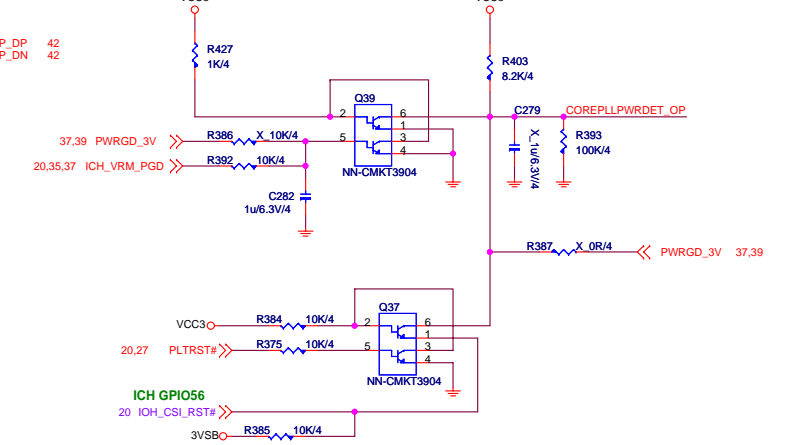
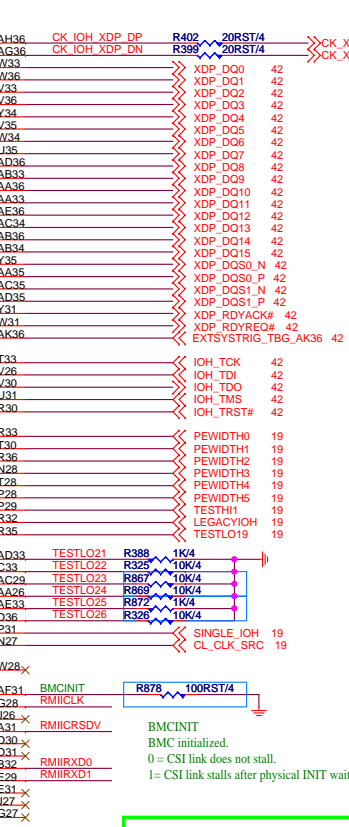
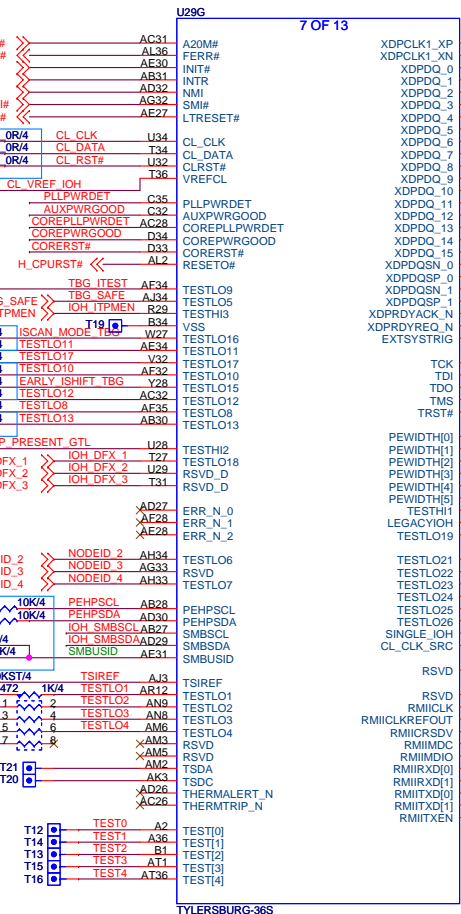
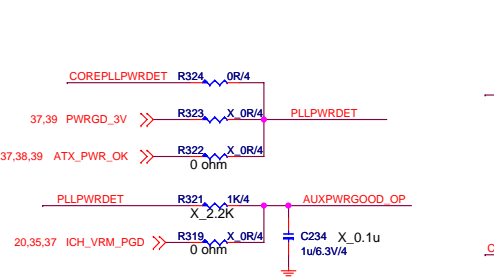




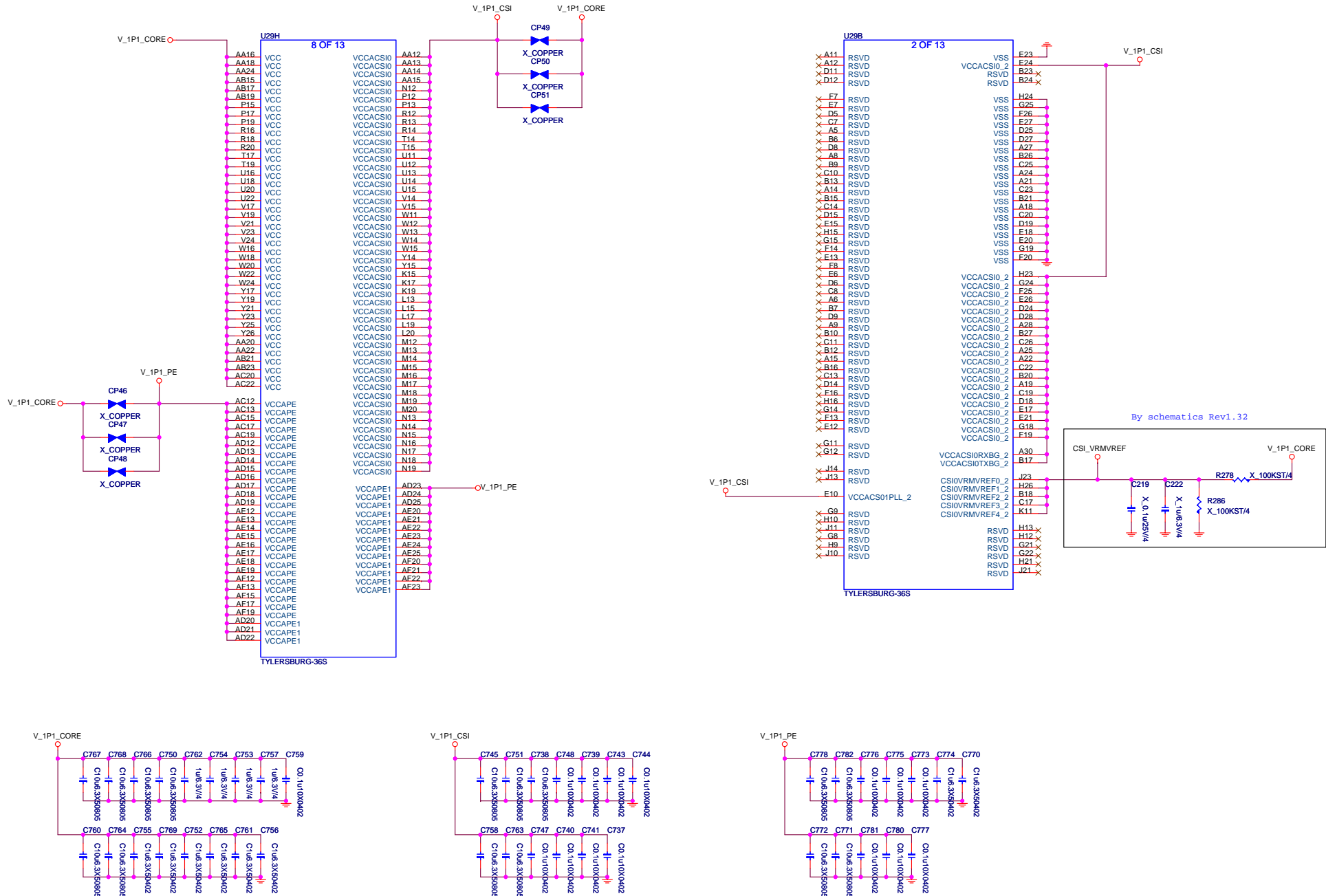


SMBUS ID:  
SMBUS ID: Indicates SMBus ID bits [7:4].  
'1' indicates an upper-address ID of 1110 (0xE).  
'0' indicates an upper-address ID of 1100 (0xC).

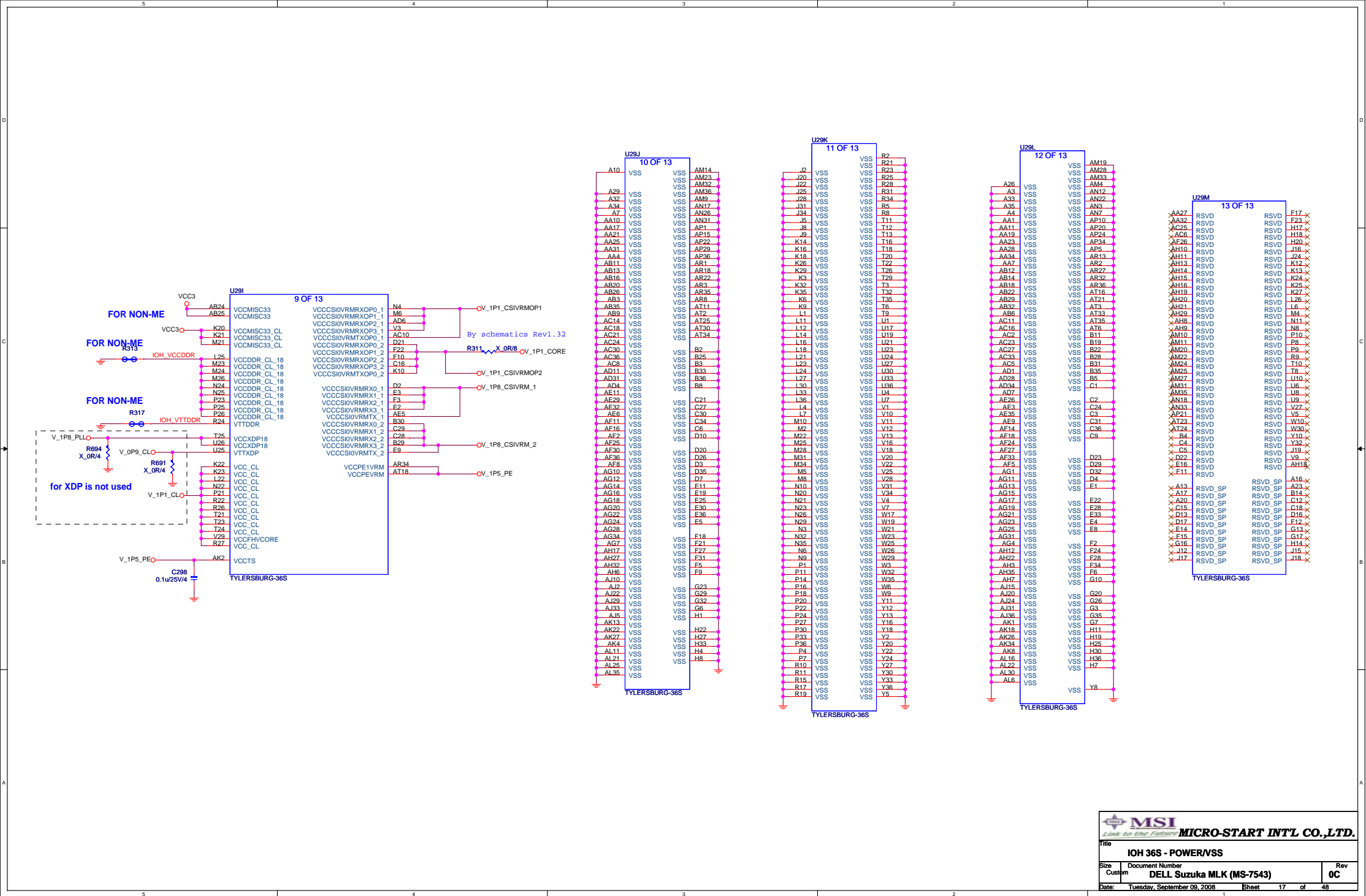
IOH SMBUSCL/SMBSDA/SMBUSID not support yet











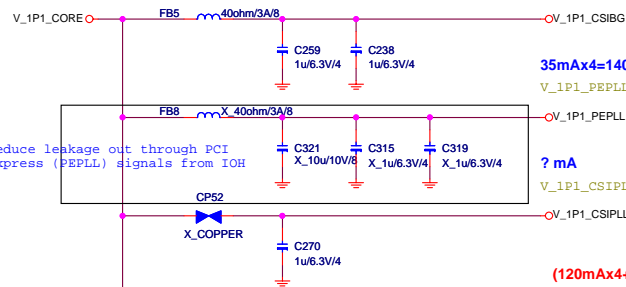


V\_1P1\_CORE REPLACE WITH V\_1P1\_VCCA

0.7A???

10mA $\times$ 2=20mA

V\_1P1\_CSIBG = CSIBG\_RX+CSIBG\_TX



35mA $\times$ 4=140mA

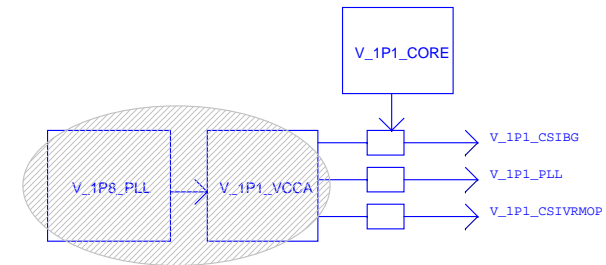
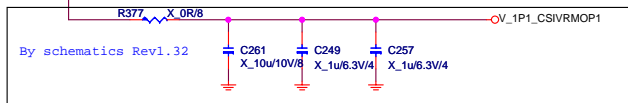
V\_1P1\_PEPLL = PEPLLA+PEPLLD

? mA

V\_1P1\_CSIPLL = CSI\_PLL

(120mA $\times$ 4+60mA)??=0.54A ?????

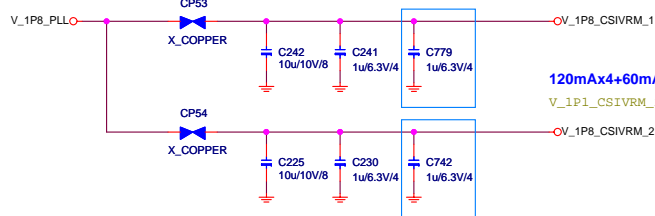
V\_1P1\_CSIVRMOP1 = CSIVRMOP\_RX[1:4]+CSIVRMOP\_TX1



1.08A

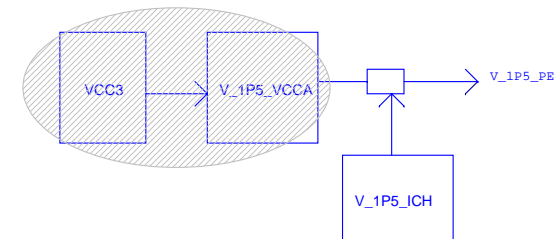
120mA $\times$ 4+60mA=0.54A

V\_1P1\_CSIVRM\_1 = CSIVRM\_RX\_1+CSIVRM1\_TX\_1



120mA $\times$ 4+60mA=0.54A

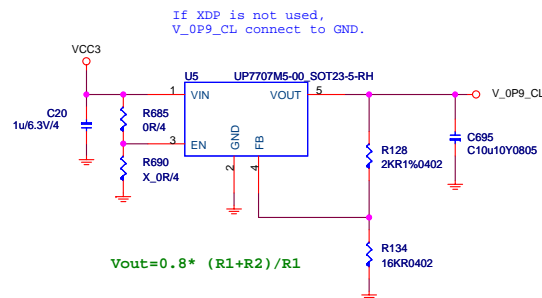
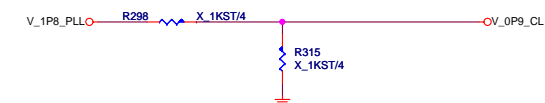
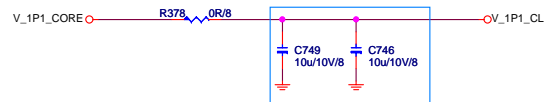
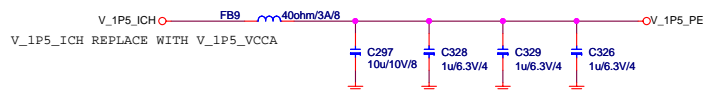
V\_1P1\_CSIVRM\_2 = CSIVRM\_RX\_2+CSIVRM1\_TX\_2



186.3mA+?

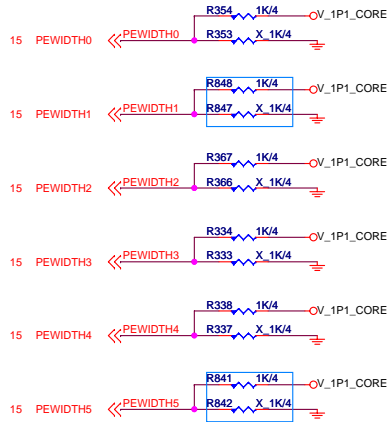
92mA $\times$ 2+1.15mA $\times$ 2+=186.3mA+?

V\_1P5\_PE = PEVRM+PEBG0+PEBG1+VCCTS

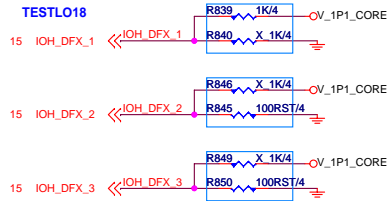




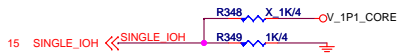
PEWIDTH0-5  
PCIE Link Width Select  
"111011" = 2x16  
"101111" = 4x8  
"011111" = Wait On Bios



IOH\_DFX\_2, 3}  
DDR frequency selection pins:  
DDRFRFREQ[3:2] as DDR frequency selection defined as:  
"00" = 133MHz input, 200MHz core  
"01" = 100 MHz input, 200MHz core  
"10" = RSVD  
"11" = RSVD



SINGLE\_IOH  
Used for dual TBG IOH selection:  
"0": IOH is not connected to another IOH on some CSI link (default)  
"1": IOH is connected to another IOH on some CSI link



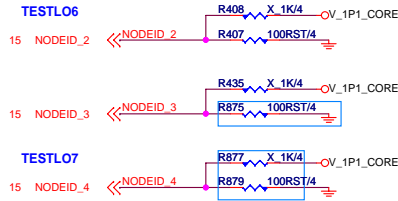
CL\_CLK\_SRC  
Used for ME default clock source:  
"1": PLL (default) -- EXT ME CLK  
"0": Ring Oscillator (back-up) -- INT ME CLK



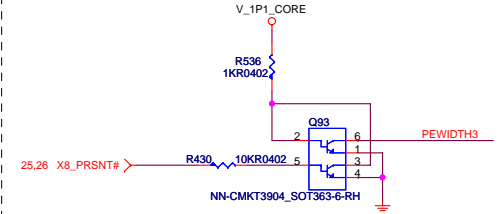
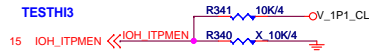
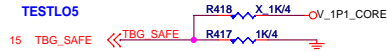
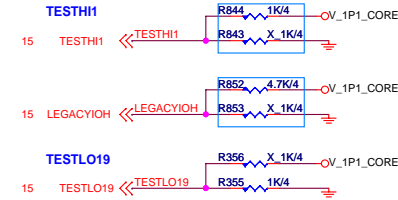
#### NON-ME FUNCTION

VCCADDRPLL and ME\_CLK\_SRC  
pins must be tied to VSS as well

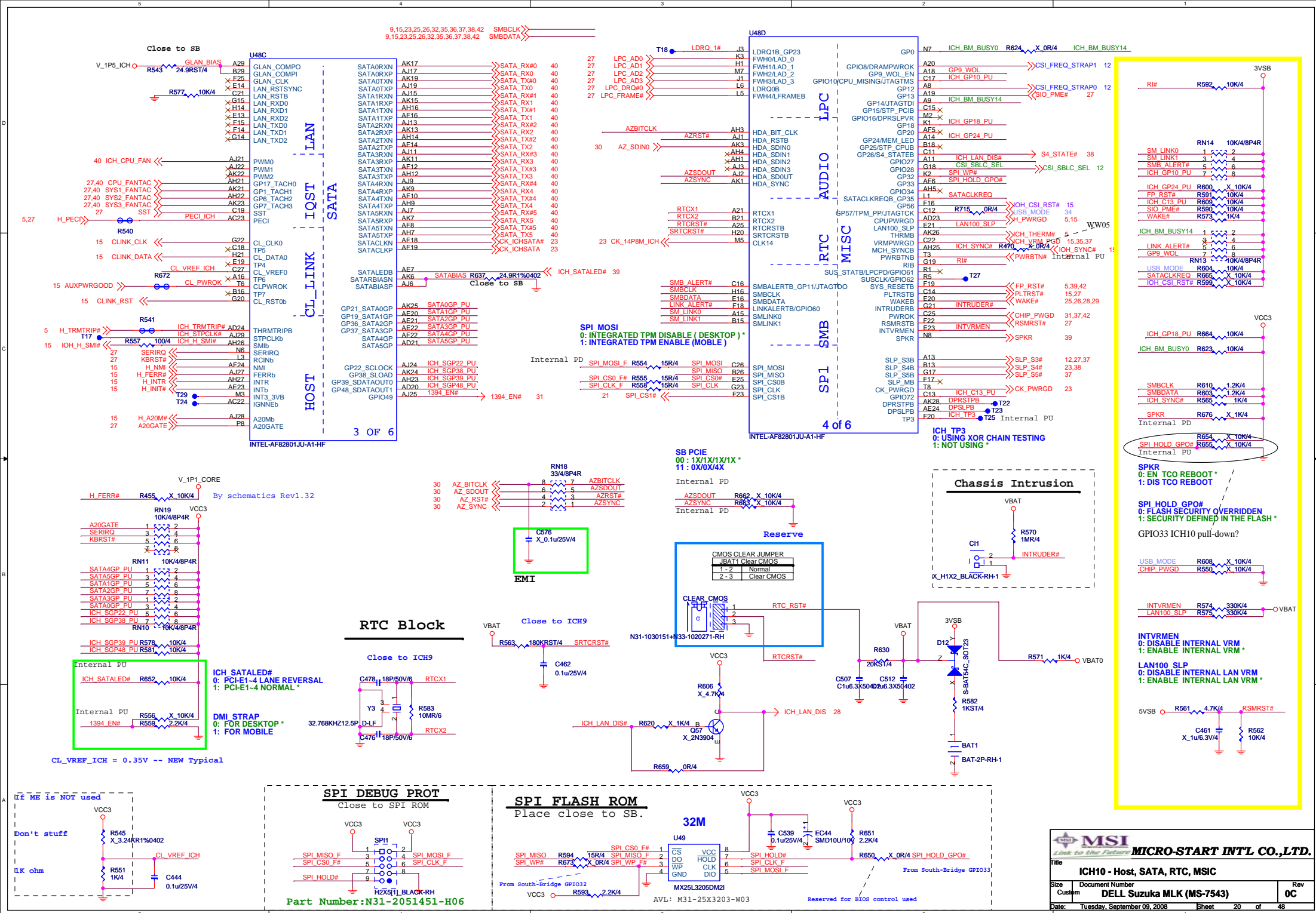
NODEID\_3\_TBG  
For dual TBG IOH configuration,  
it indicates which CSI port is connected to the other IOH.  
"0": CSI0  
"1": CSI1



LEGACYIOH  
Used to determine legacy or non-legacy selection:  
"1": Legacy IOH  
"0": Non-legacy IOH





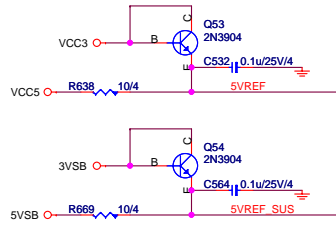




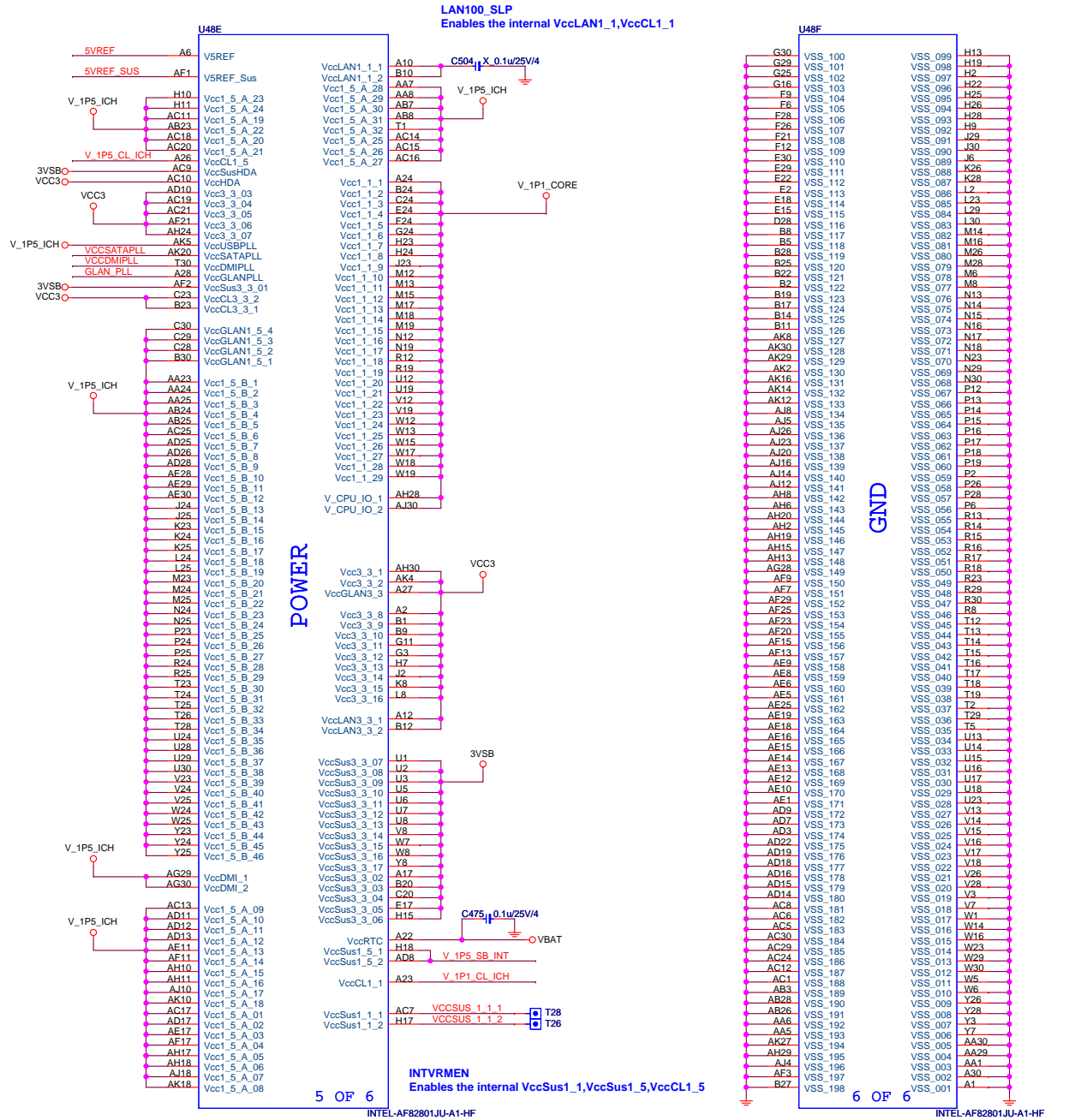
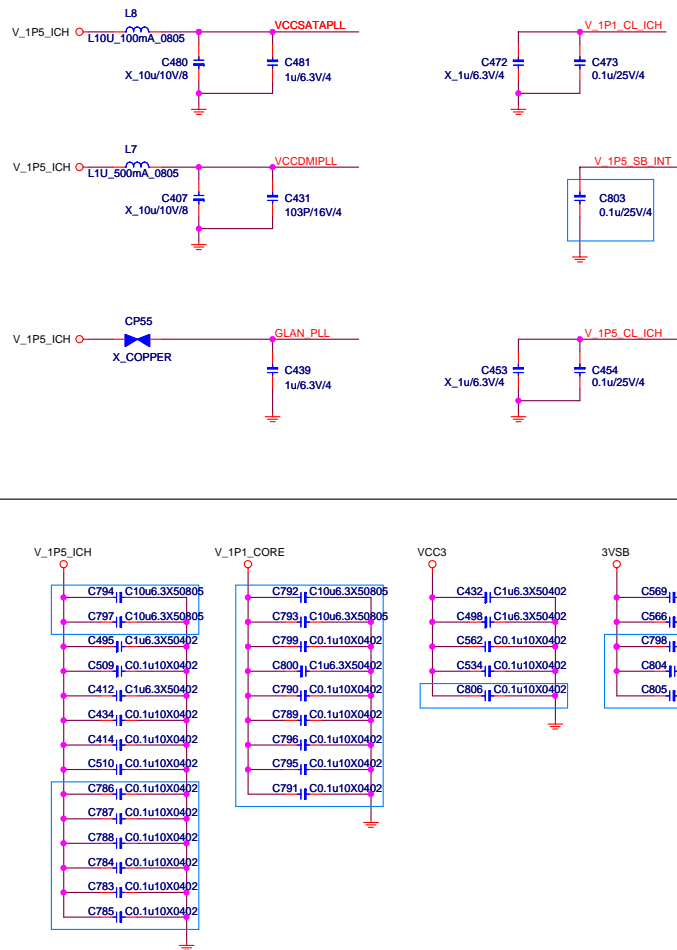




## 5VREF & 5VREF\_SUS Sequencing Circuit

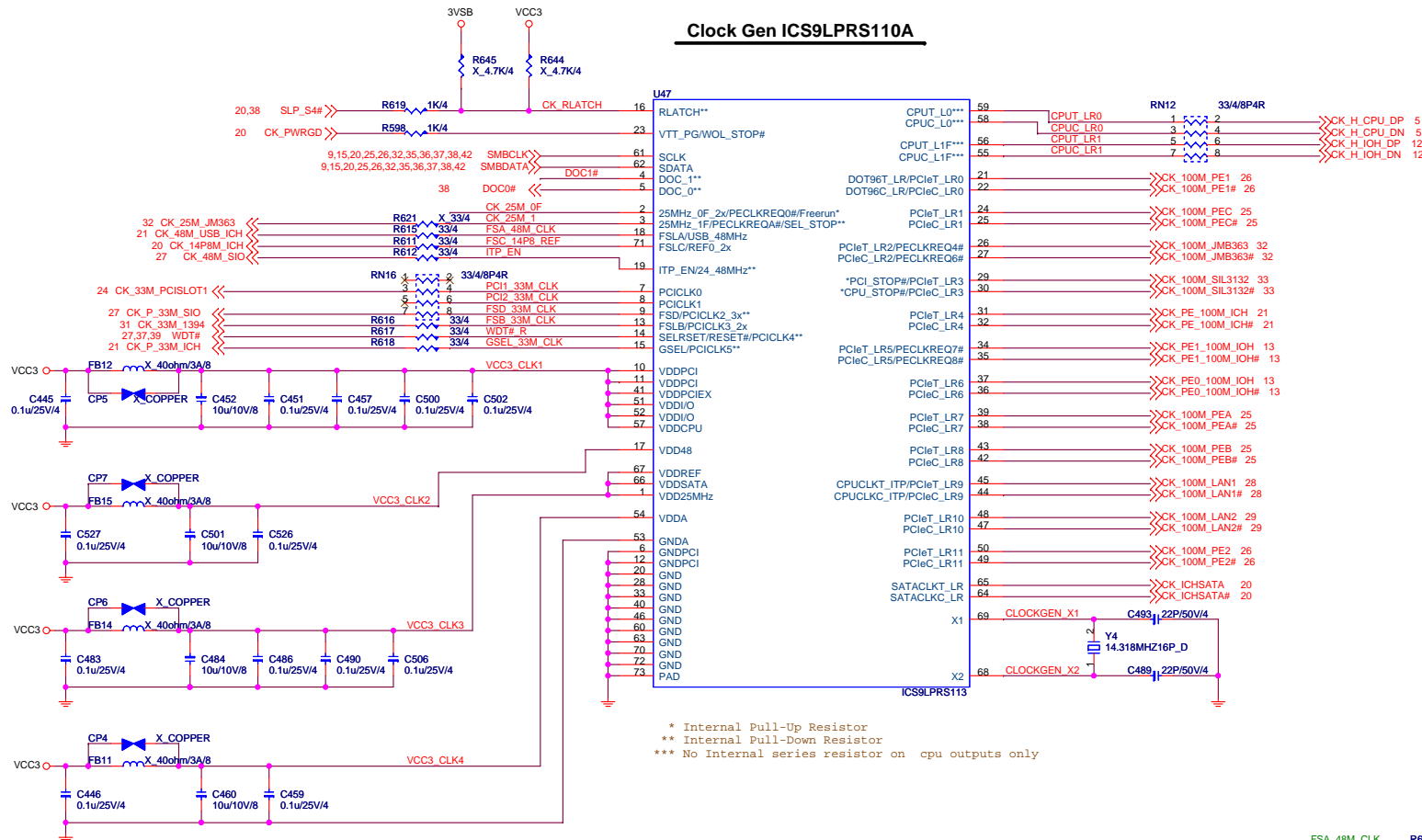


## SB POWER

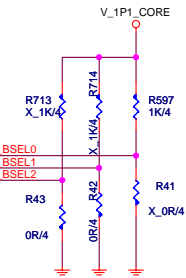
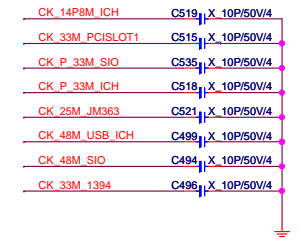
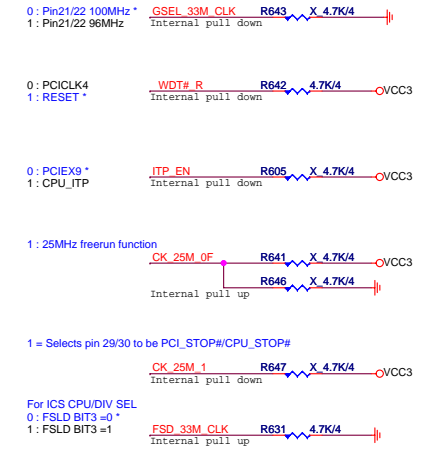




## Clock Gen ICS9LPRS110A



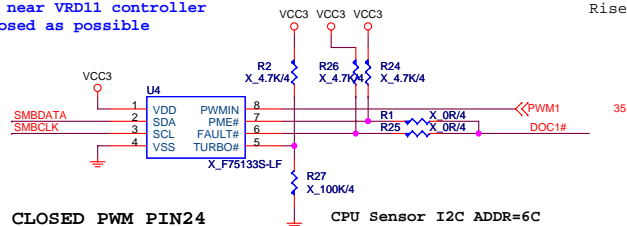
## CLOCK GEN STRAPING



BSEL	TABLE
2 1 0	FSB FREQUENCY
0 0 0	266 MHz
0 0 1	133 MHz ( default )
0 1 0	200 MHz
0 1 1	166 MHz
1 0 0	333 MHz
1 0 1	100 MHz
1 1 0	400 MHz
1 1 1	200 MHz

## EASY DOT FUNCTION

Place near VRD11 controller as closed as possible

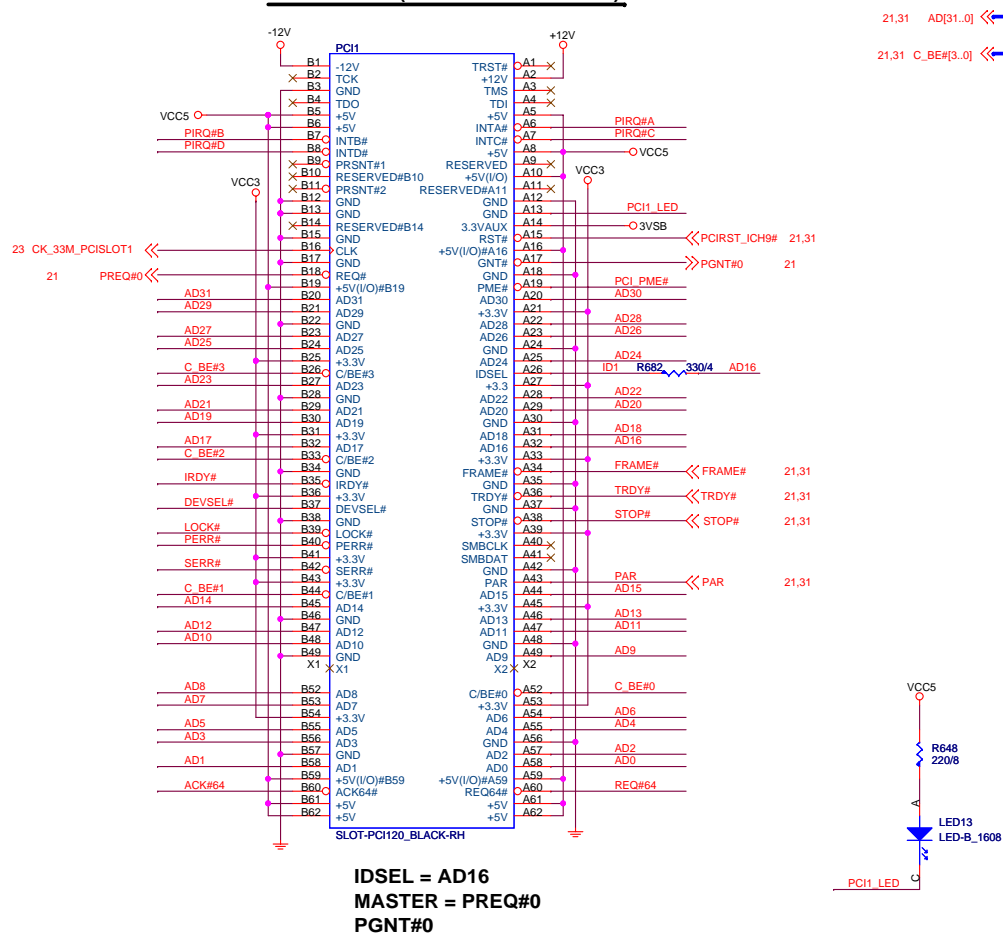


Vimon= (Riout / N) x (Rx/Risen) x Iload  
 Riout = Rimon  
 Rx = DCR  
 Risen = ISEN+

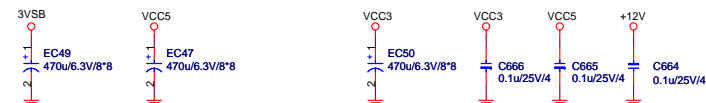
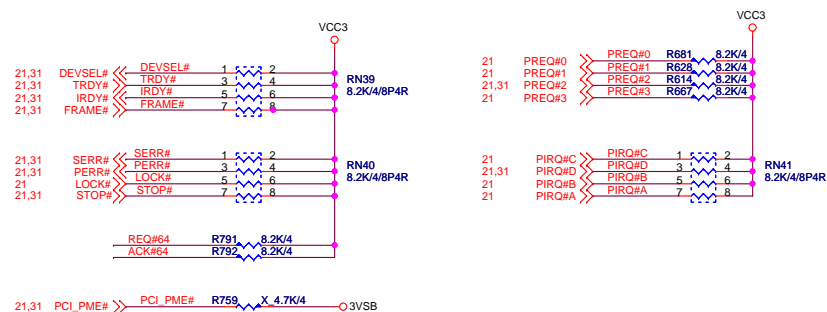
DOC#0	DOC#1	Over-clk
1	1	15%
0	1	10%
1	0	5%
0	0	Normal



**PCI SLOT 1 (PCI VER: 2.2 COMPLY)**

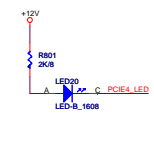
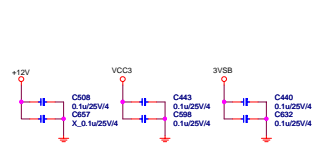
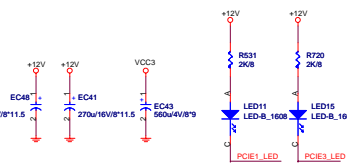
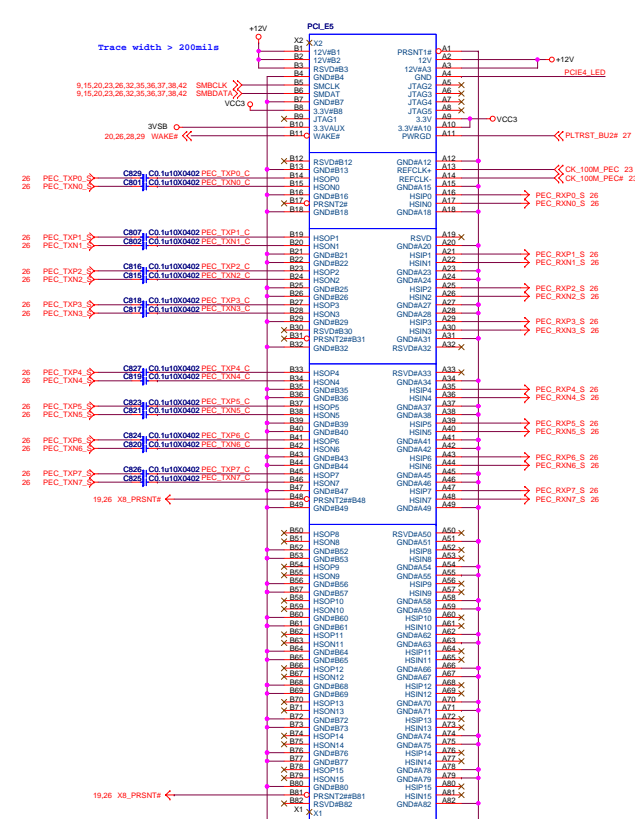
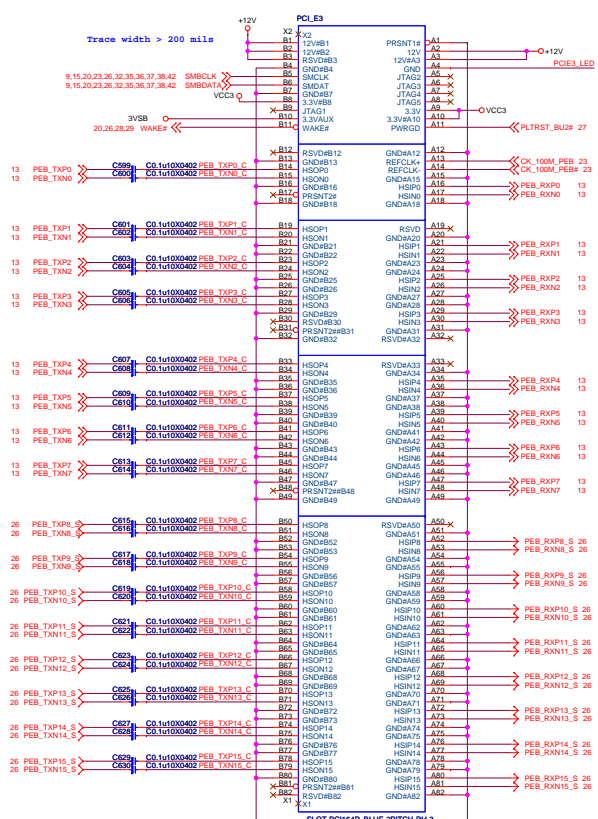
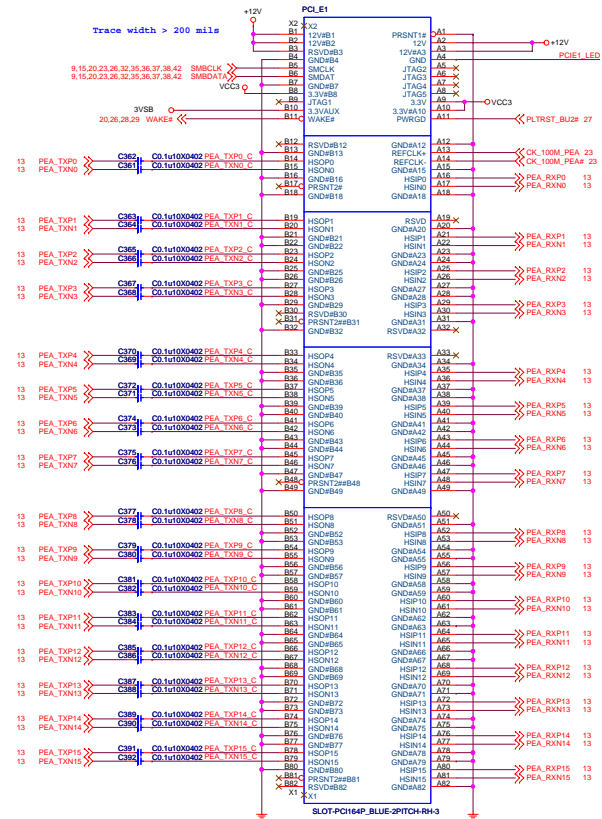


## PCI PULL-UP / DOWN RESISTORS





PCI\_Express X16 SLOT1,2,3



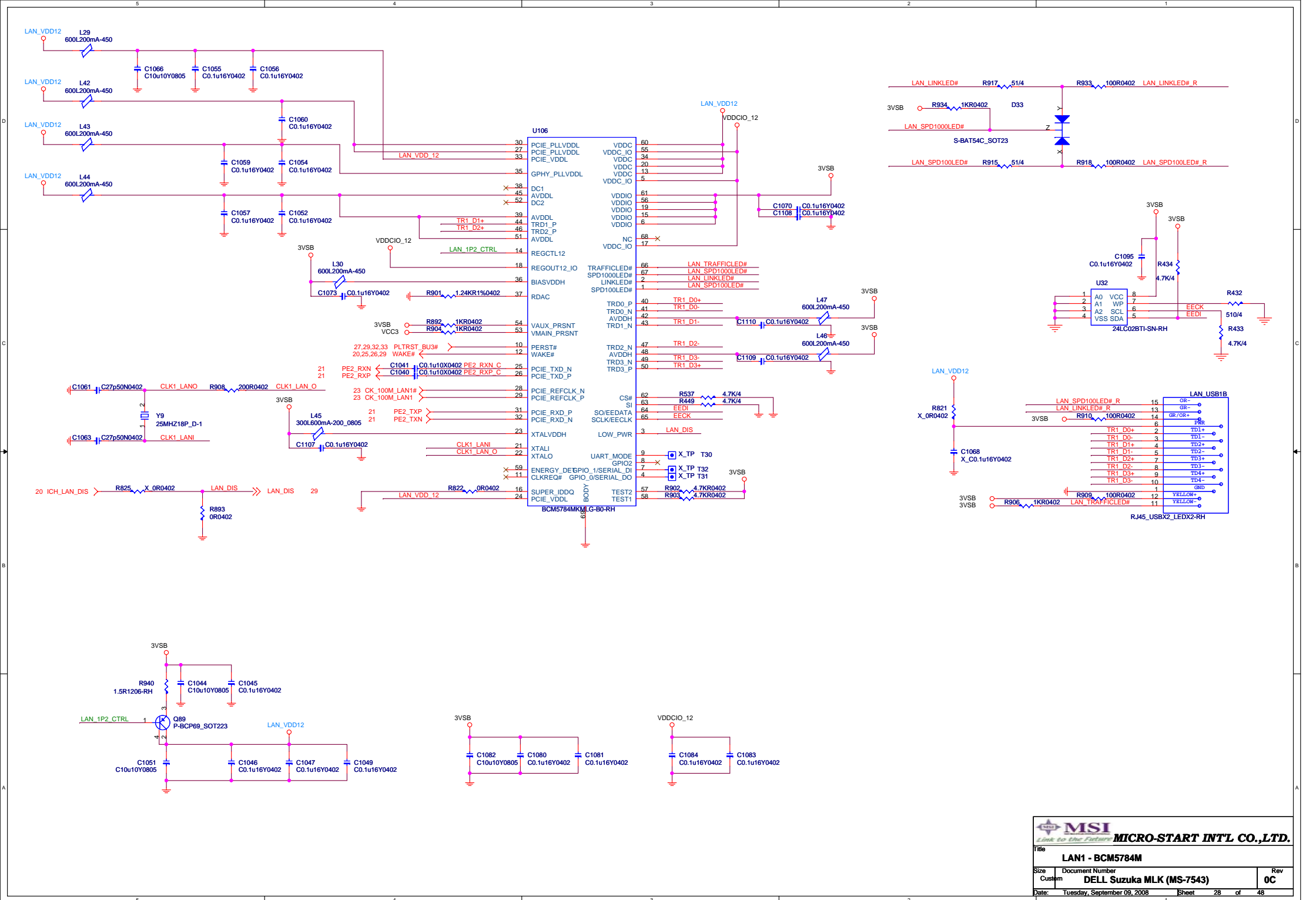




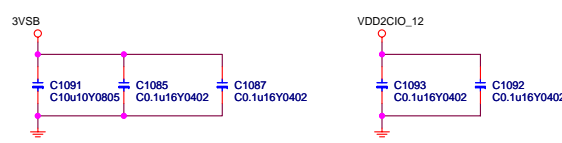
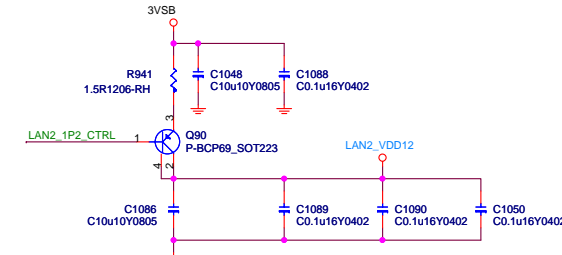
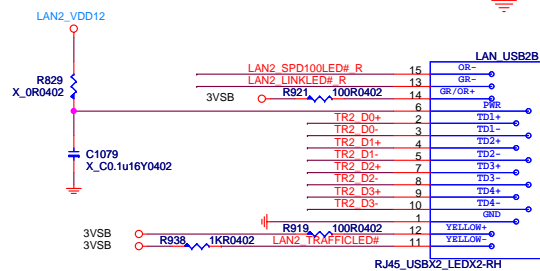
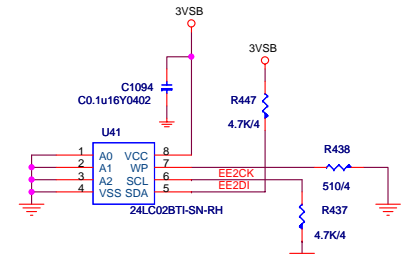
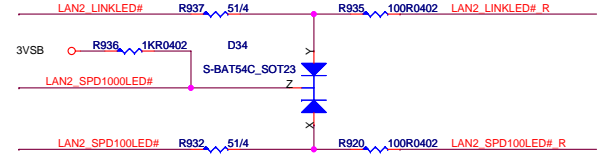
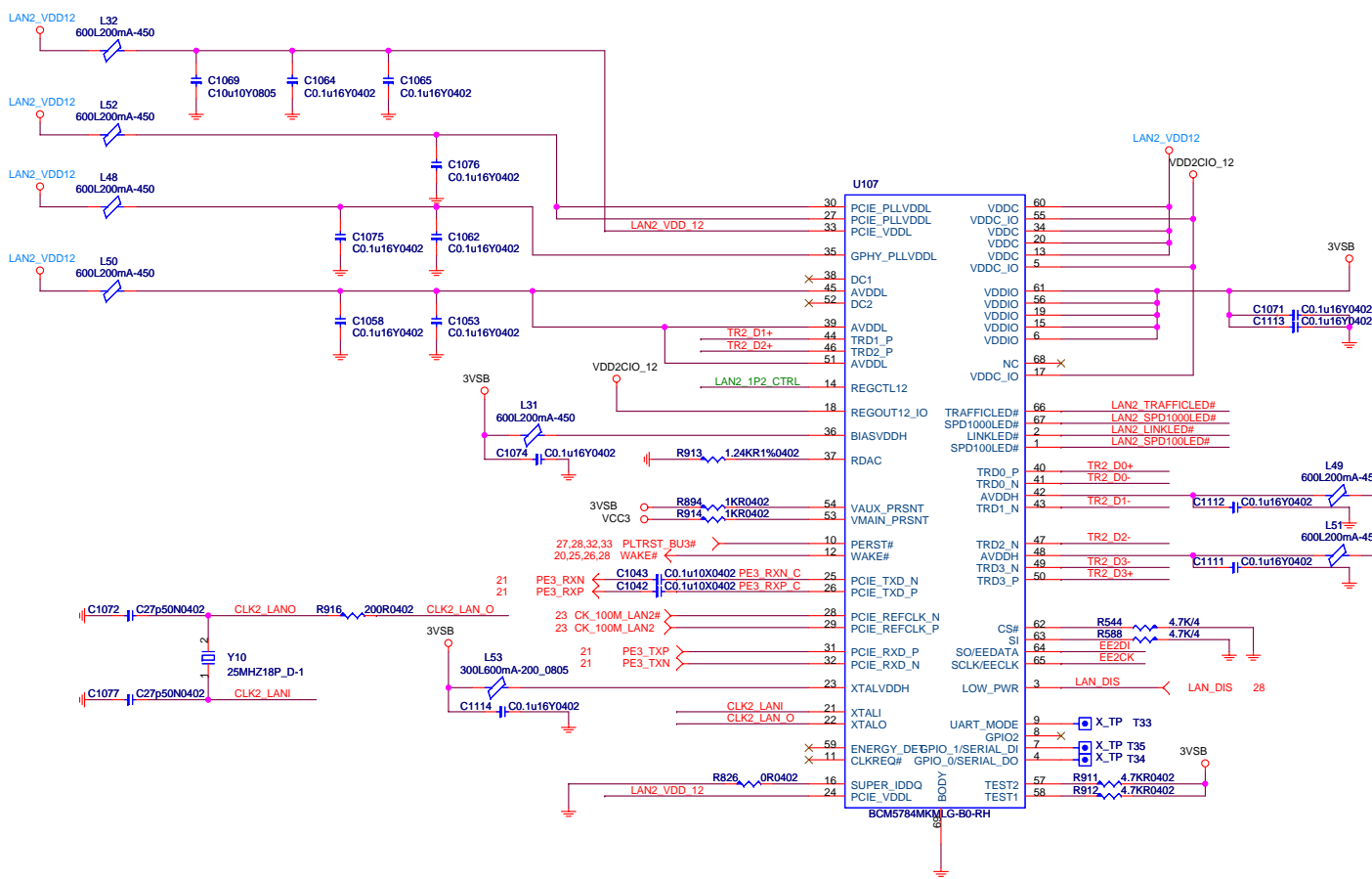




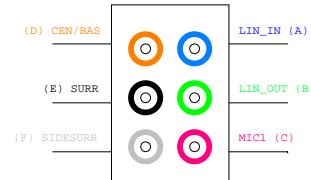
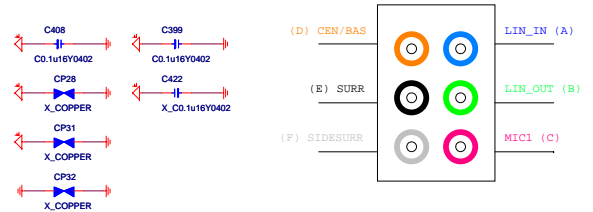
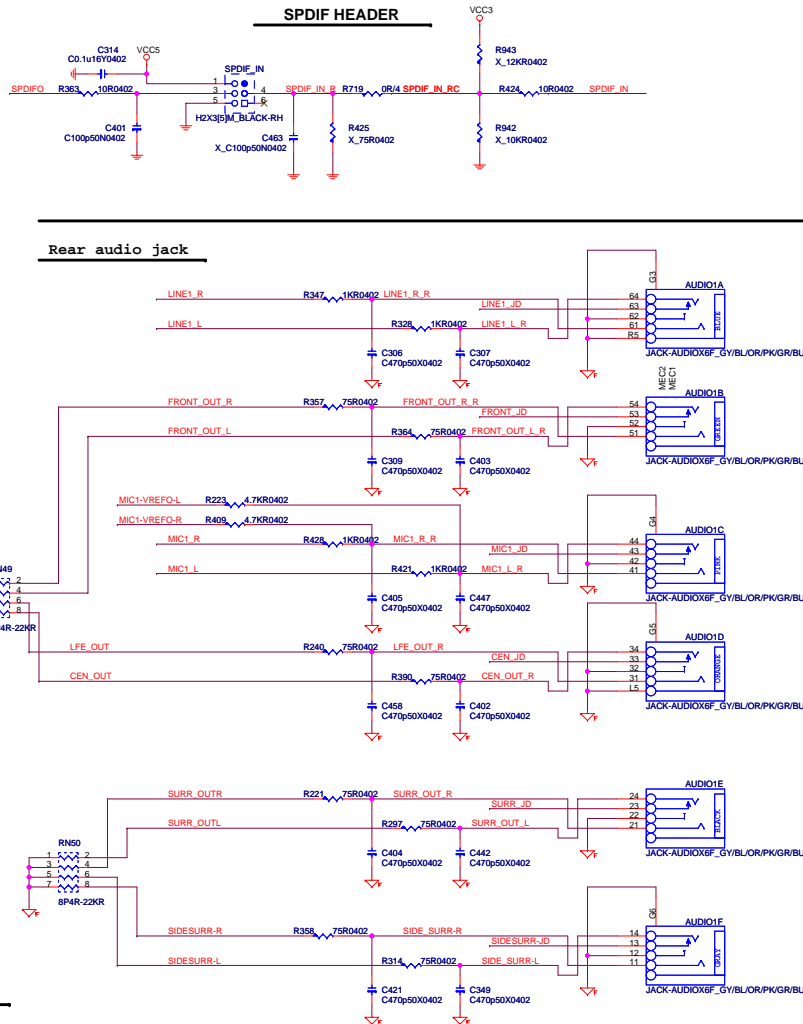
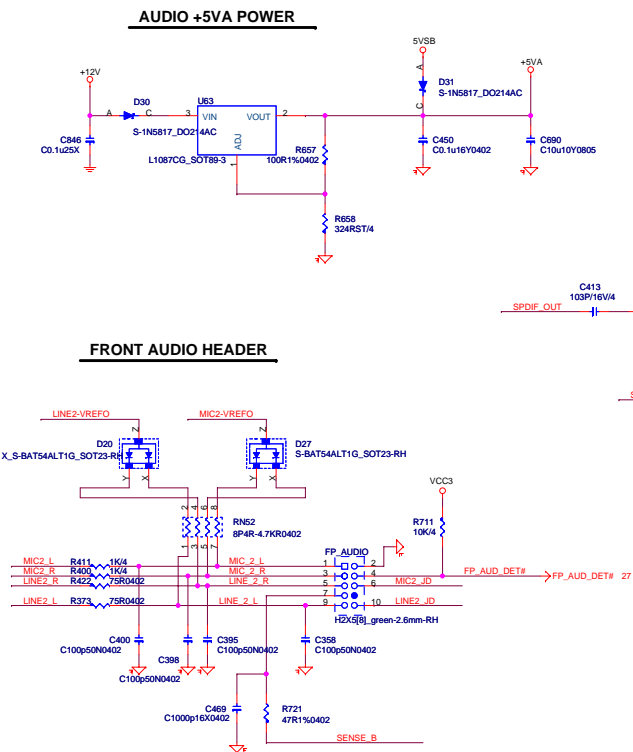
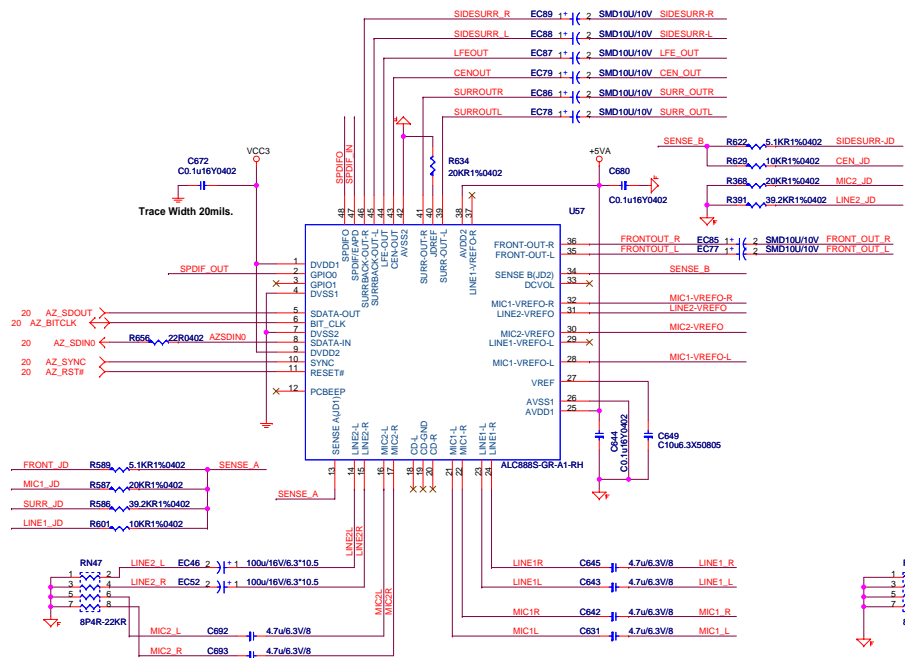






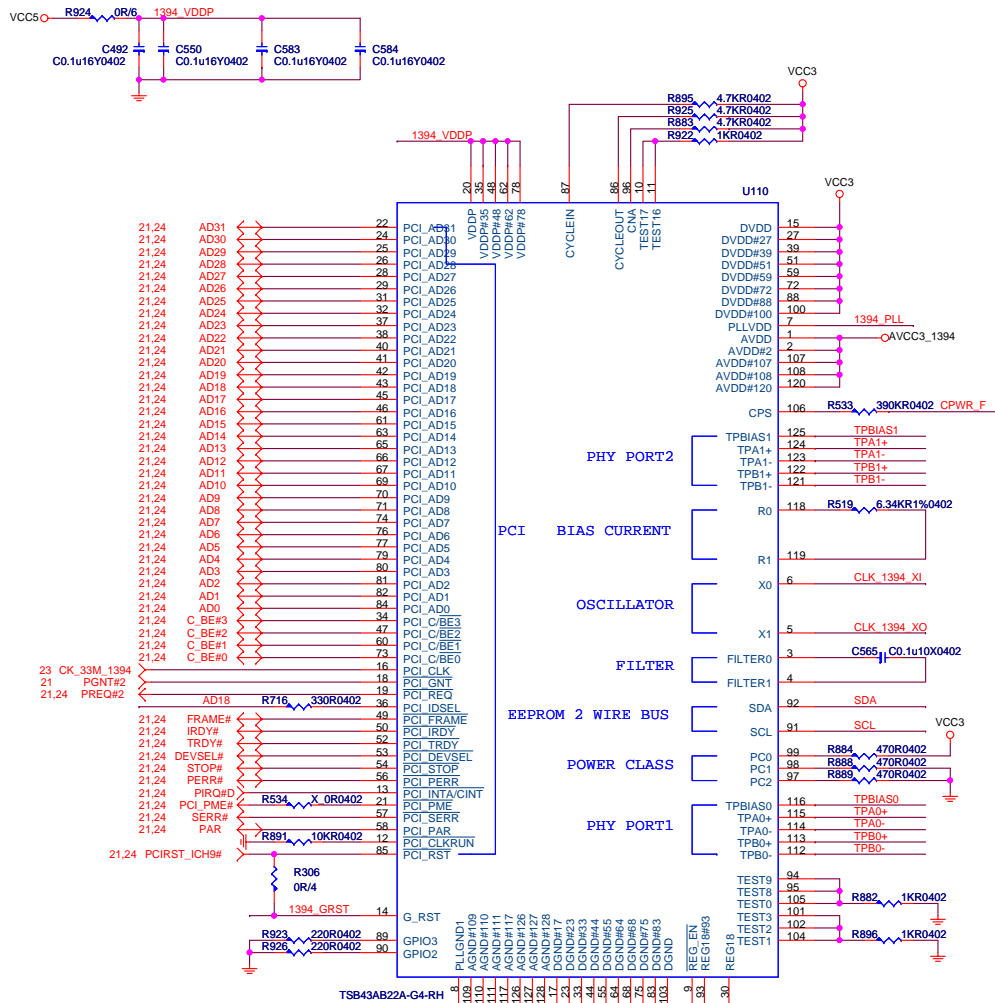








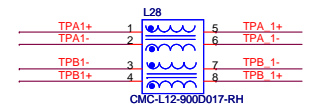
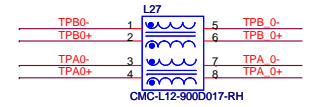
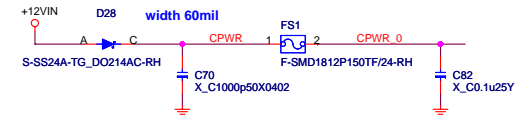
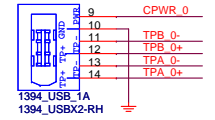
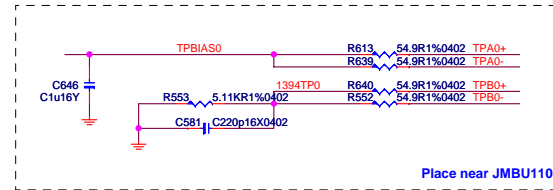
## 1394 CONTROLLER



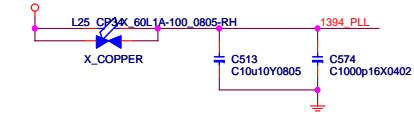
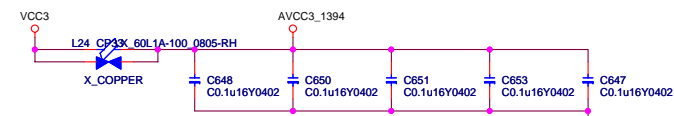
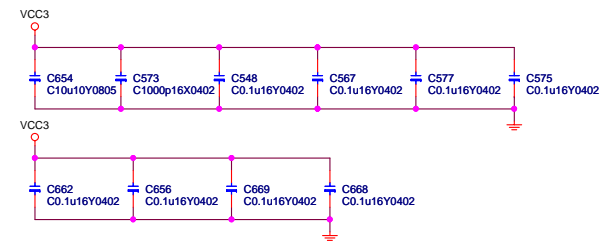
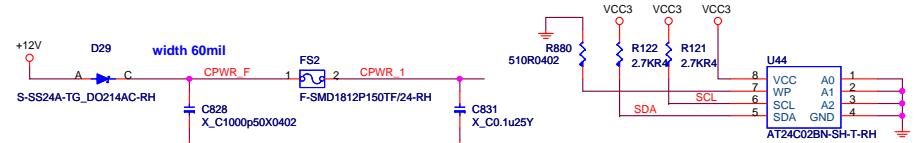
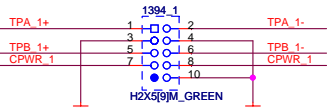
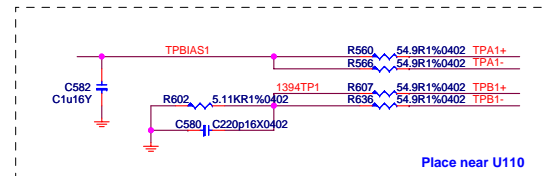
```

IDSEL = AD18
MASTER = PREQ#2
PGNT#2

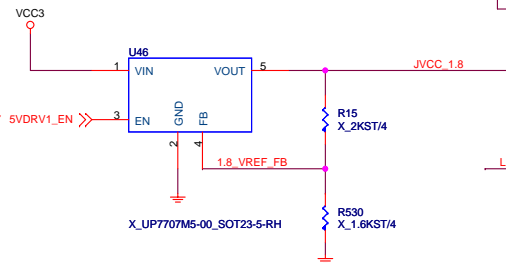
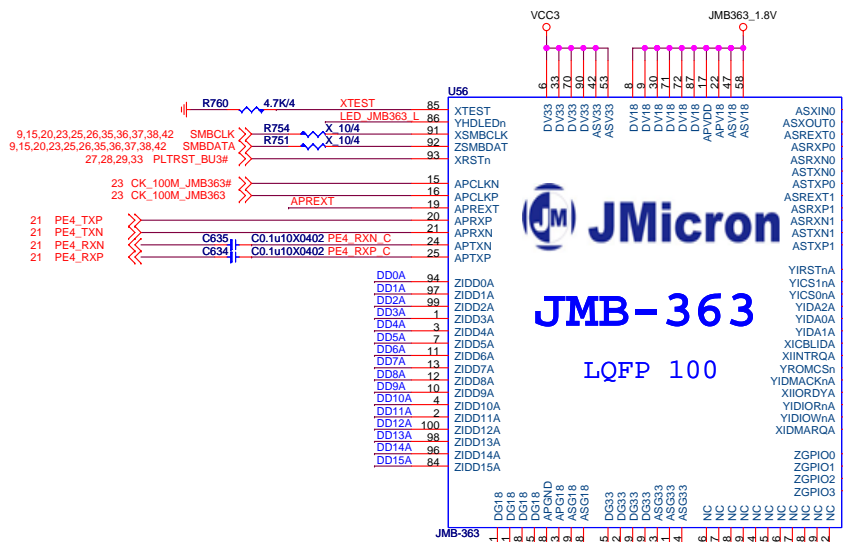
```

Rear 1394 port

Front 1394 pin header

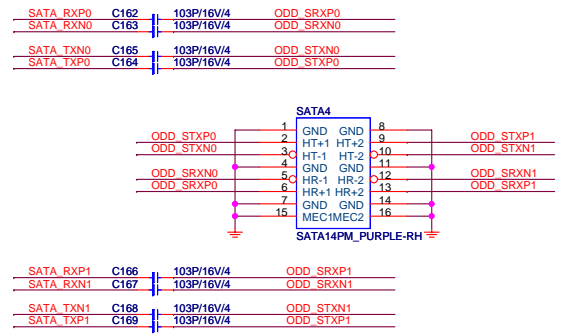




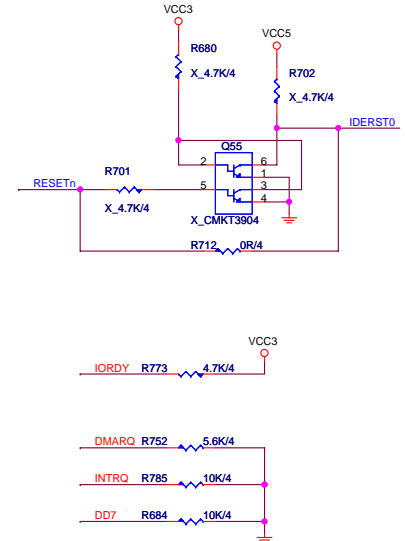


UP7707  
 $V_{OUT} = 0.8 \times (R1 + R2) / R1$

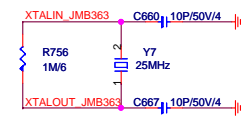
2S



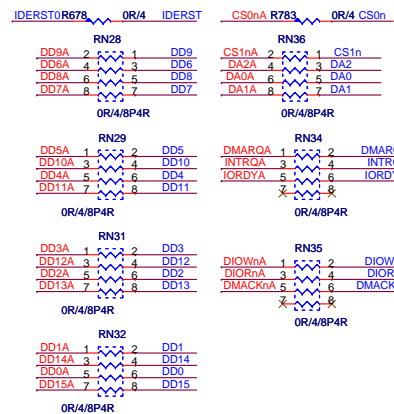
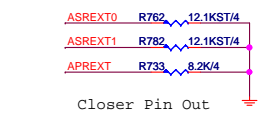
1P



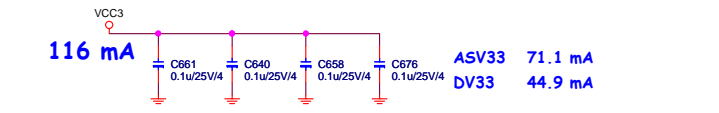
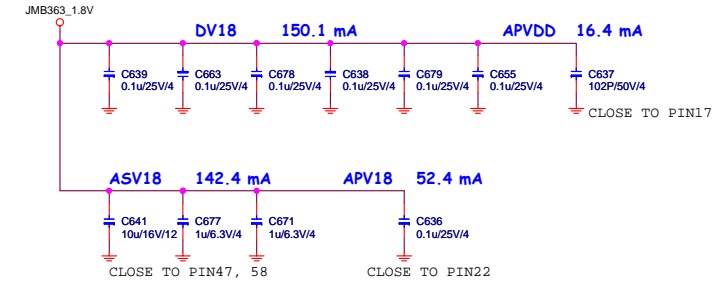
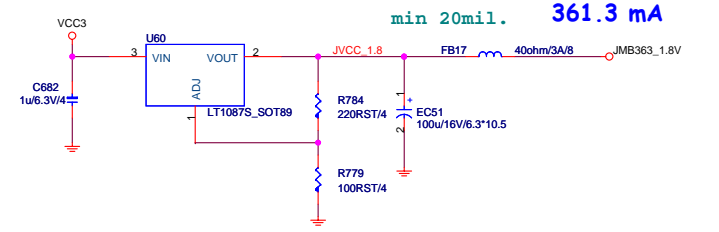
GPIO1 is clock source  
 0: from internal clock source  
 1: from ASXIN & ASXOUT



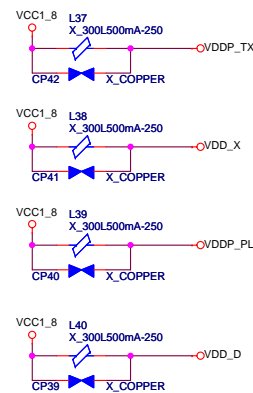
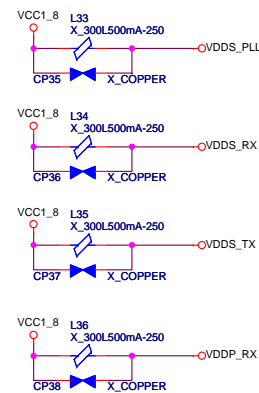
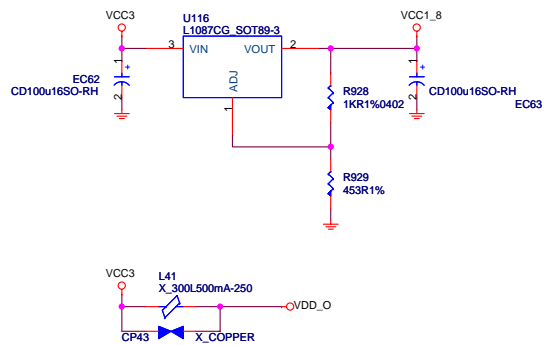
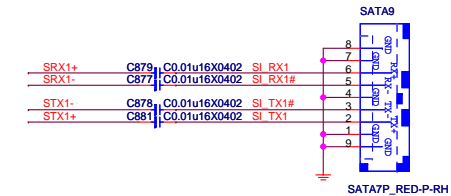
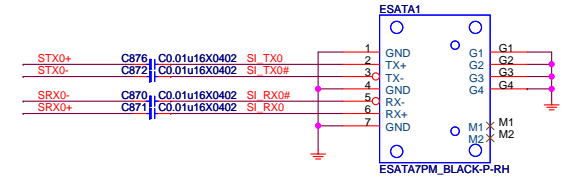
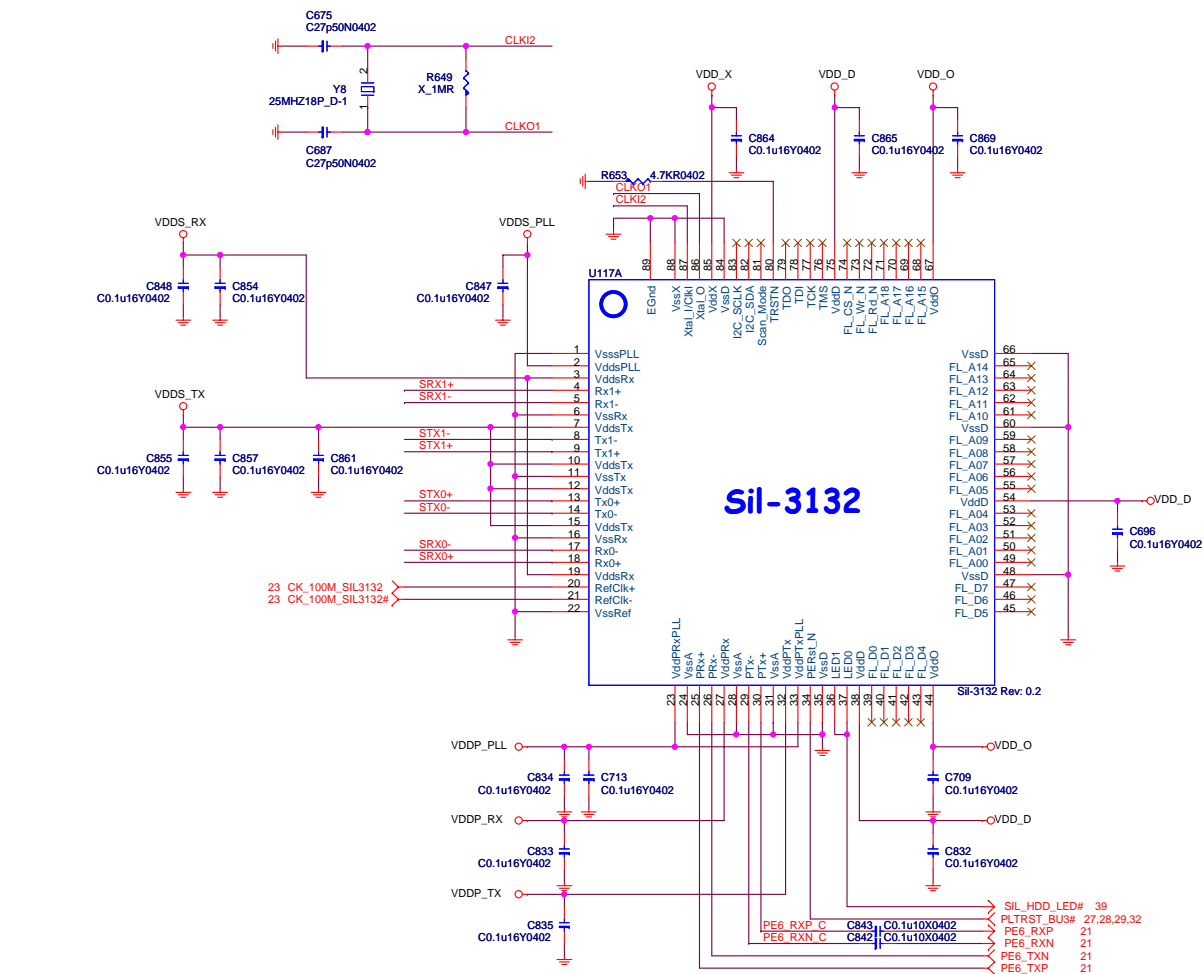
XTAL: 50ppm is recommend.



if the length of JMB-363 to IDE connector more than 4inch, that must stuff damping resistor.

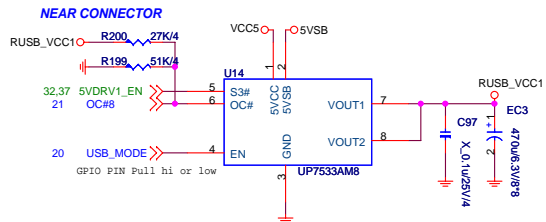




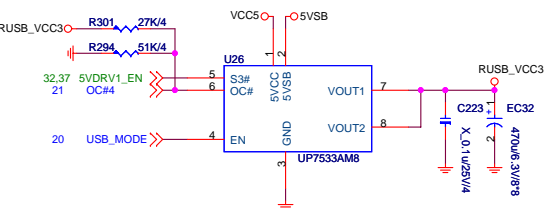




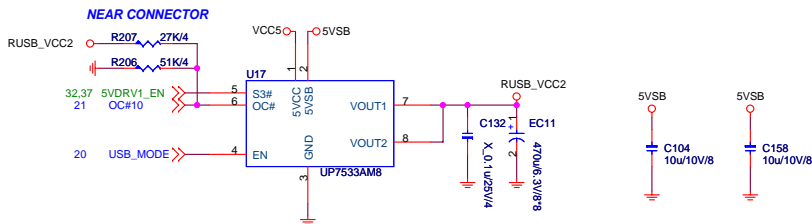
## USB POWER FOR PORT 0,1



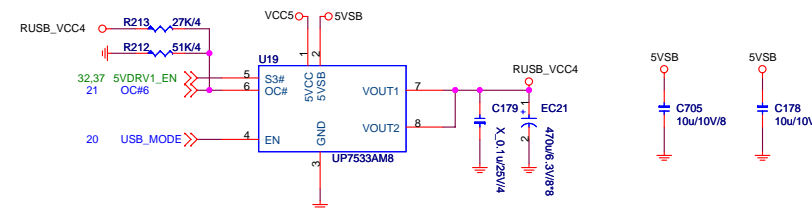
## USB POWER FOR PORT 4, 5



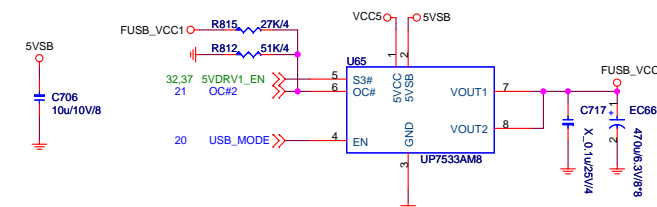
## USB POWER FOR PORT 2,3



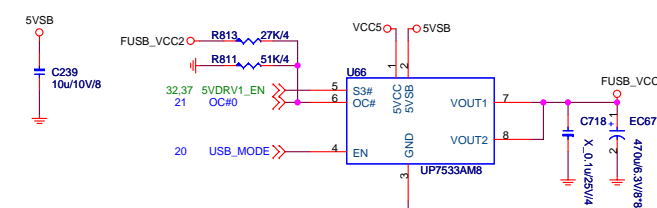
## USB POWER FOR PORT 6,7



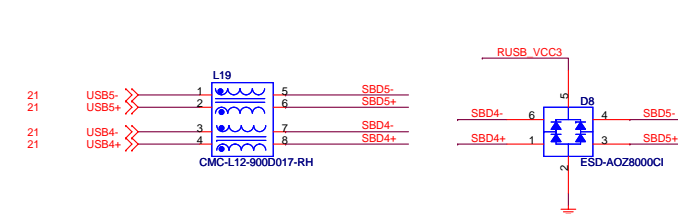
## USB POWER FOR PORT 8,9



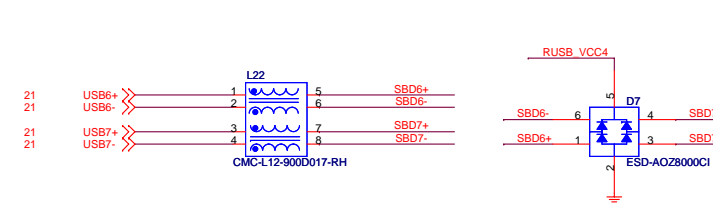
## USB POWER FOR PORT 10,11



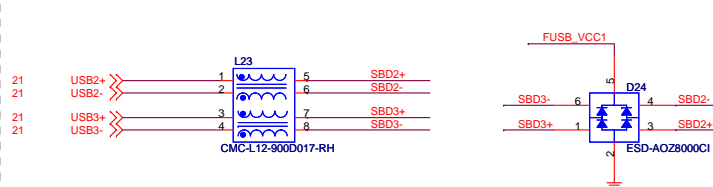
## REAR USB PORT 4,5 (With LAN)



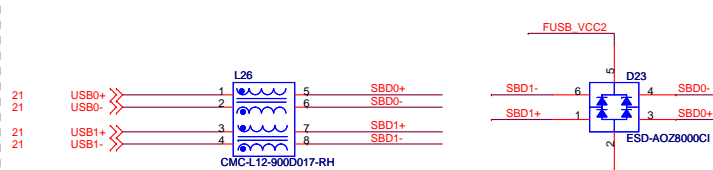
## REAR USB PORT 6,7 (With LAN)



## FRONT USB PORT 8,9

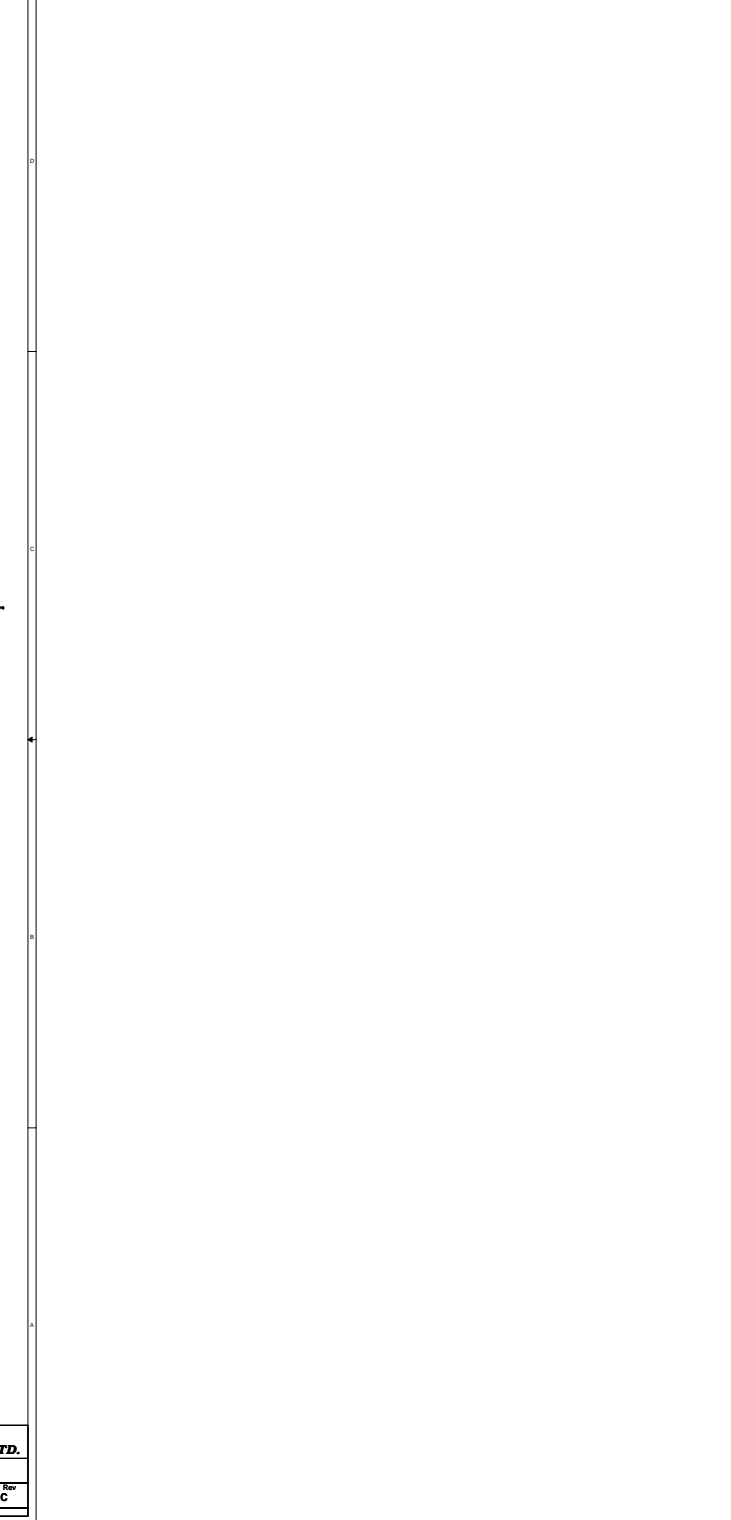
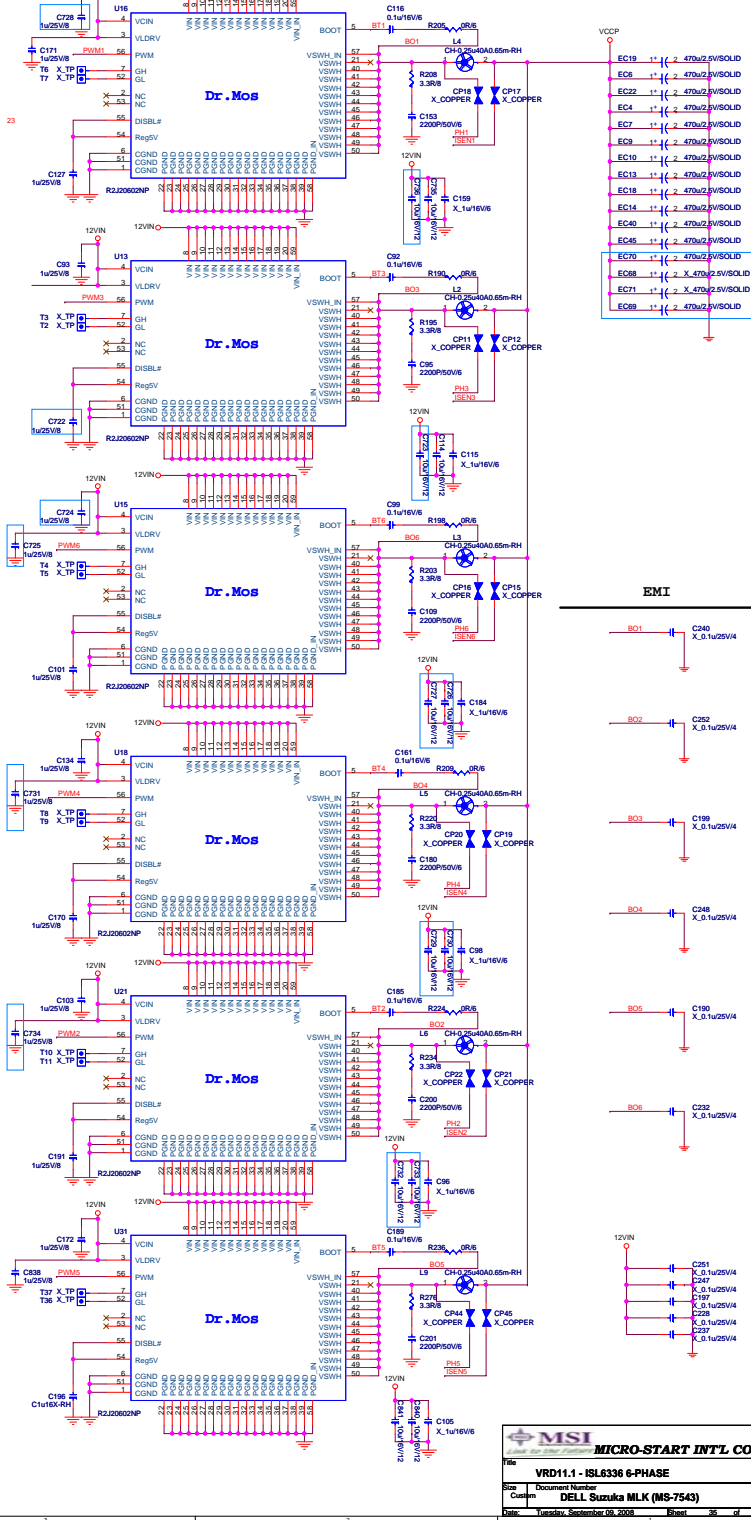
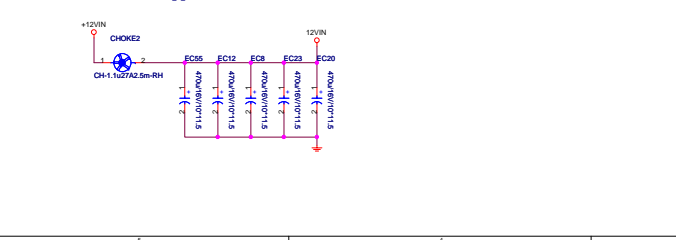
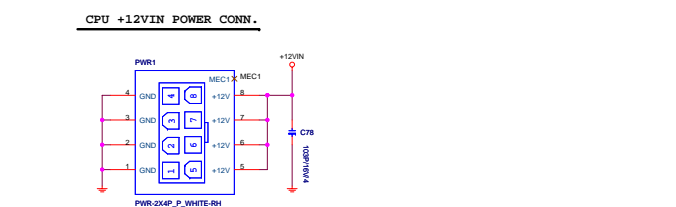
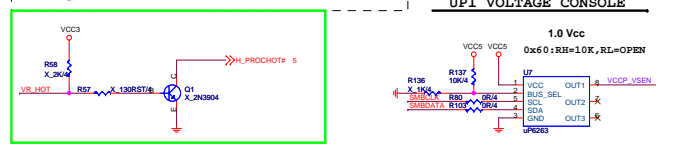
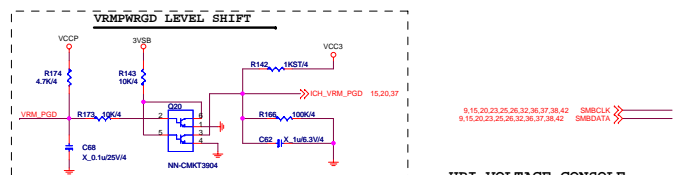
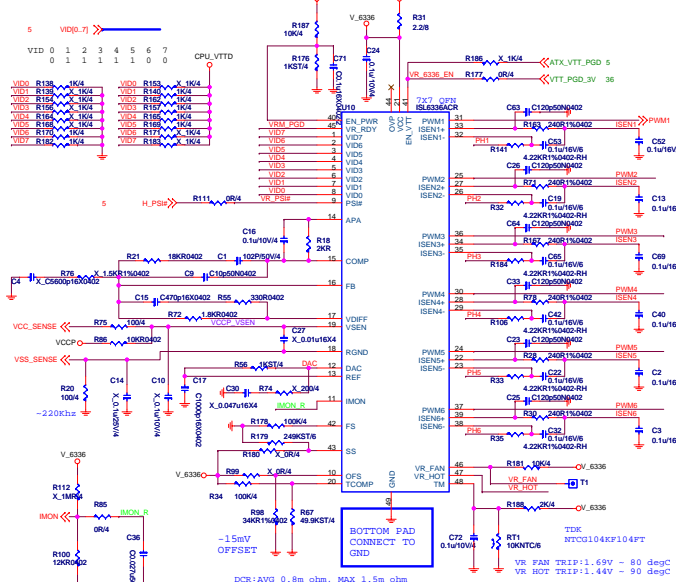


## FRONT USB PORT 10,11



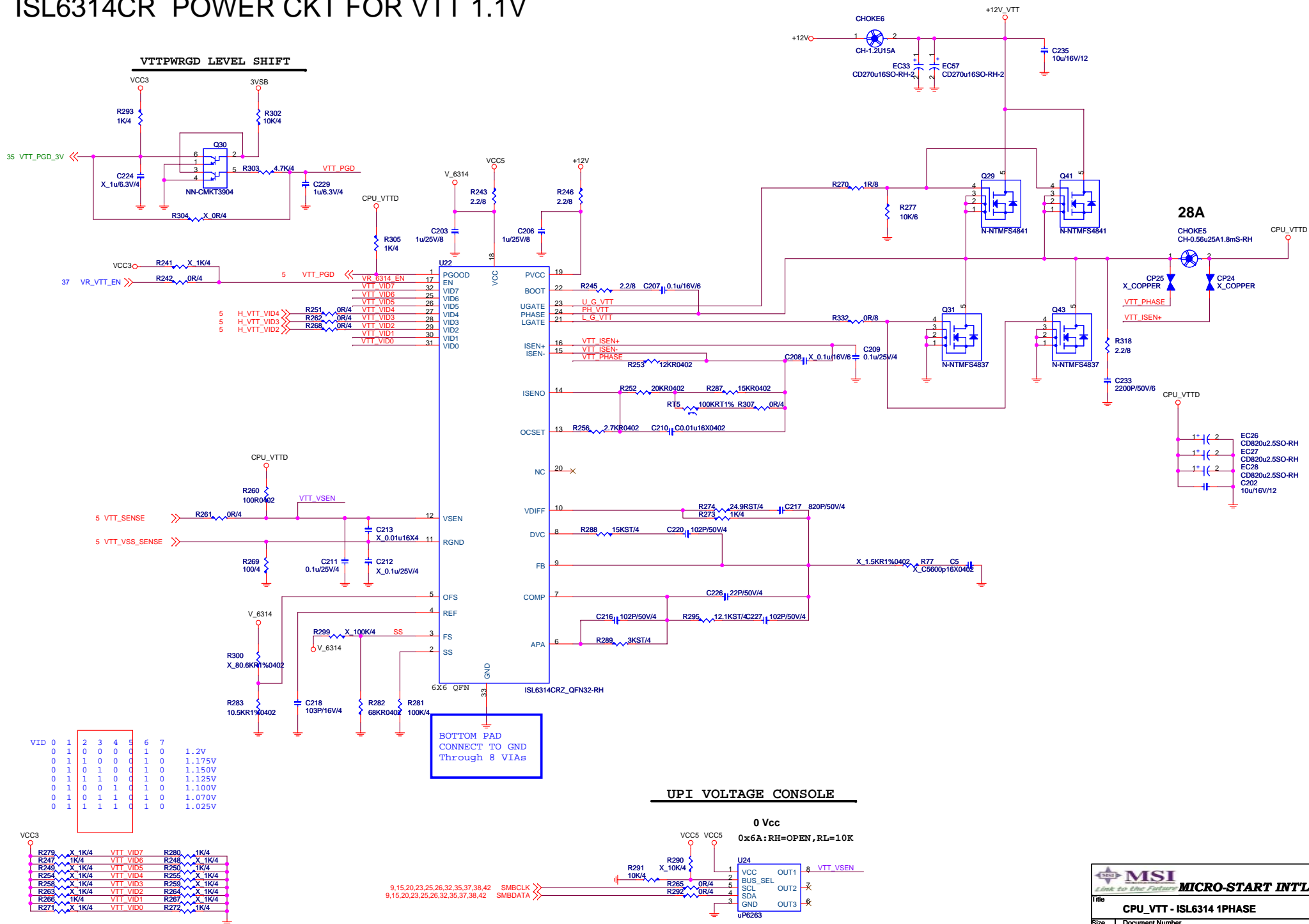


### ISL6336CR VRD11.1 POWER CKT





## ISL6314CR POWER CKT FOR VTT 1.1V

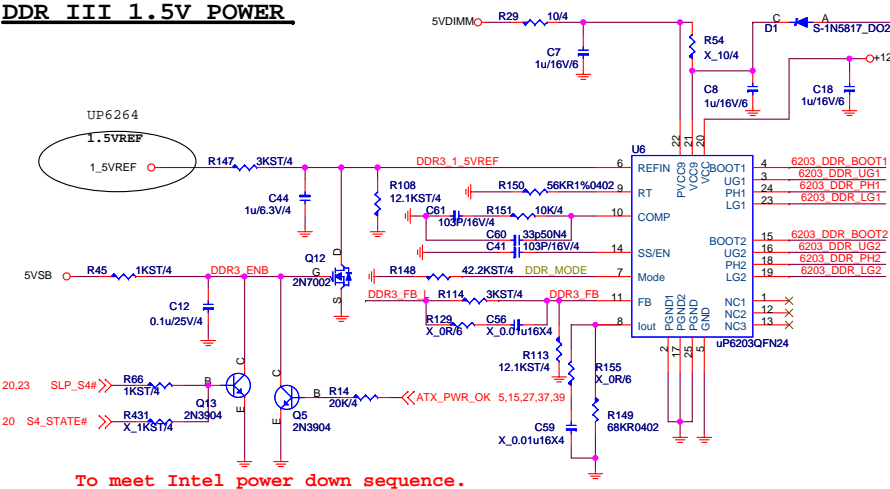




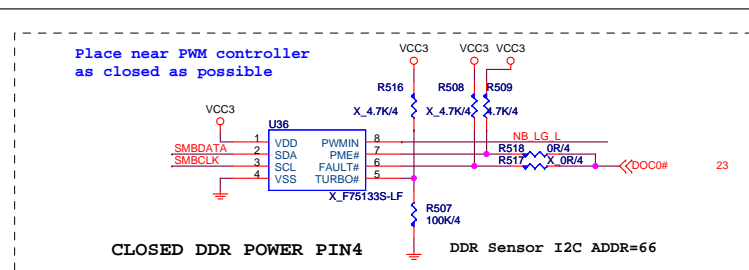




## DDR III 1.5V POWER



To meet Intel power down sequence.



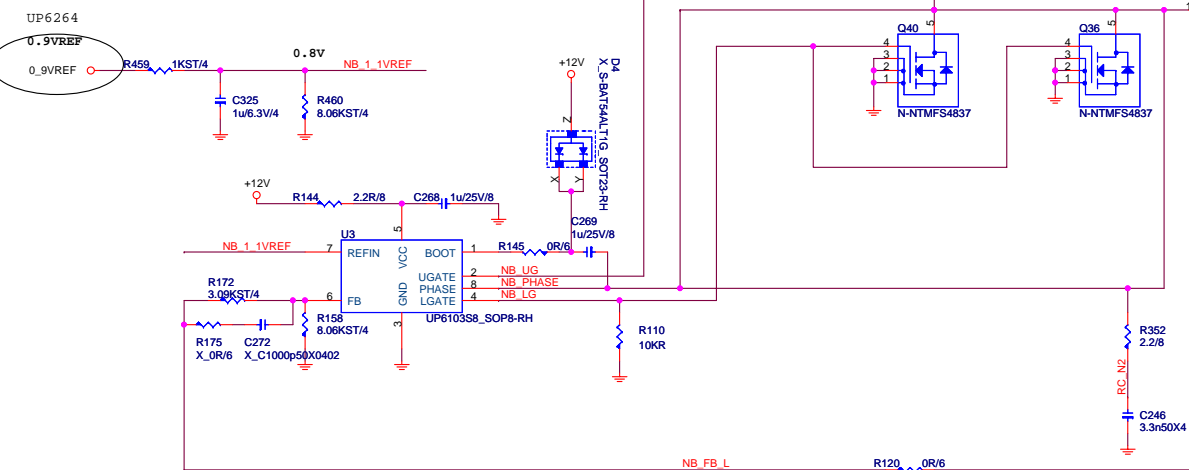
CLOSED DDR POWER PIN4

-----

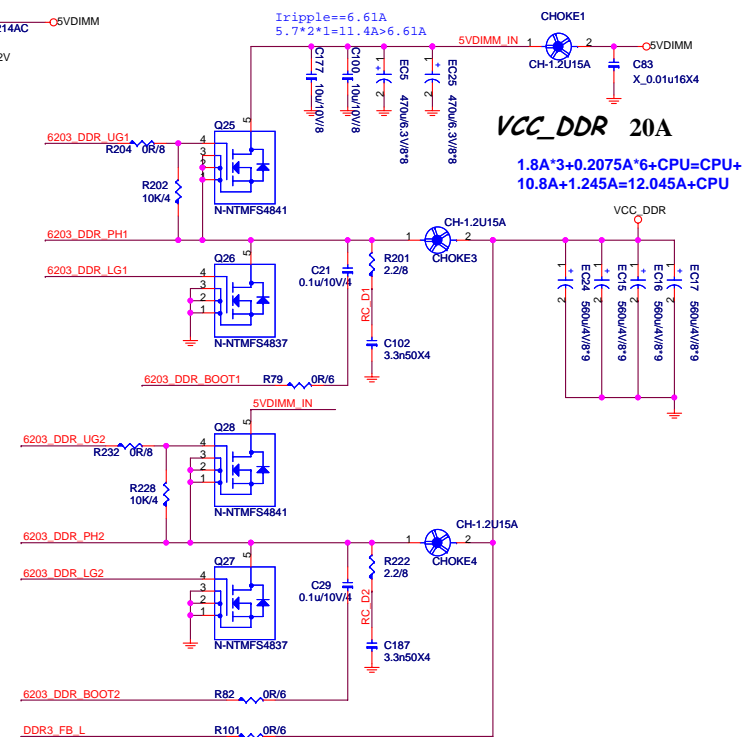
1,15,20,23,25,26,32,35,36,37,42 SMBDATA

1,15,20,23,25,26,32,35,36,37,42 SMBCLK

NB 1.1V POWER



--	--

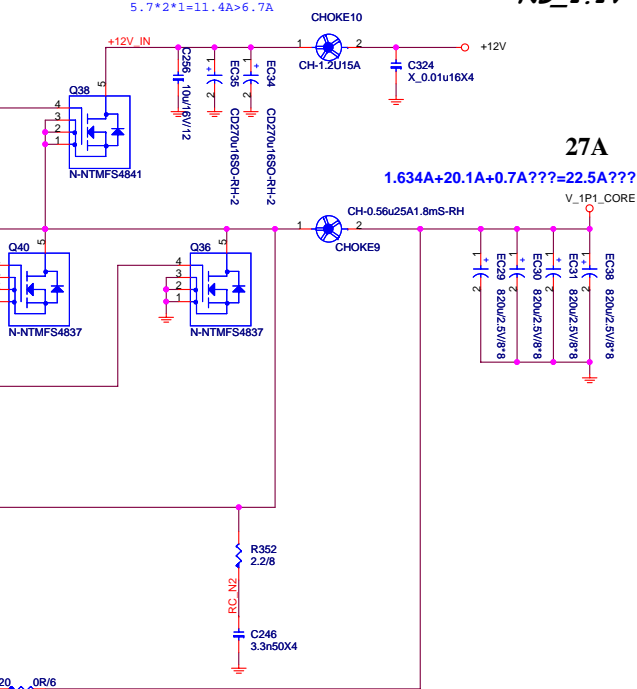


**VCC\_DDR 20A**

$$1.8A^3 + 0.2075A^6 + CPU = CPU + 10.8A + 1.245A = 12.045A + CPU$$

$I_{ripple} = 6.7A$   
 $5.7 * 2 * 1 = 11.4A > 6.7A$

***NB 1.1V***

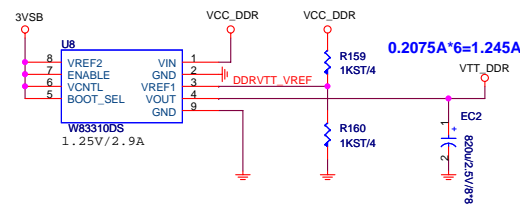


**27A**

$1.634A + 20.1A + 0.7A = 22.5A$

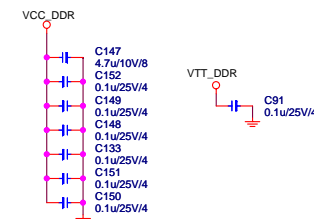
### DDR VTT Power

To CPU Copper trace width > 250mils , Fill island behind DIMM > 400mils .


$$0.2075A \cdot 6 = 1.245A$$

VR TO DIMM SOCKET

### LDO TO DIMM SOCKET

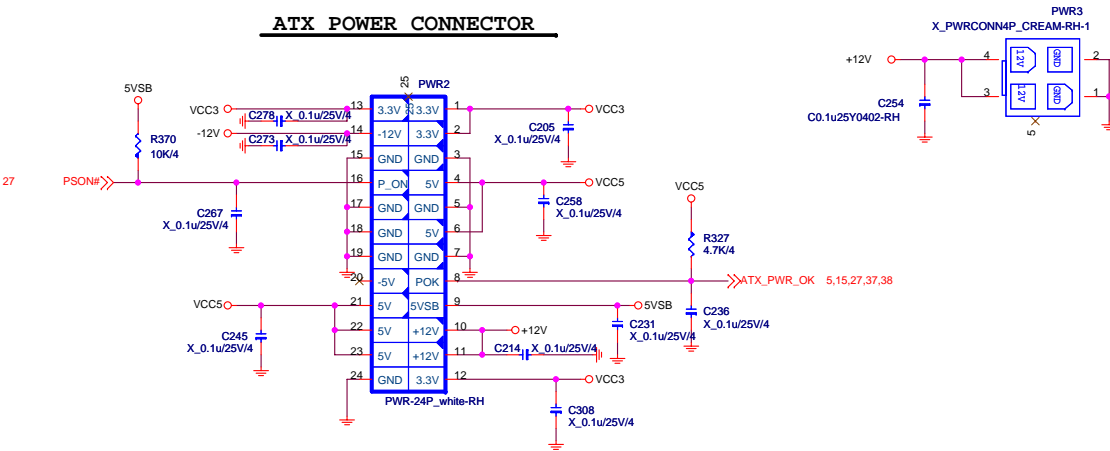


VTT\_DDR

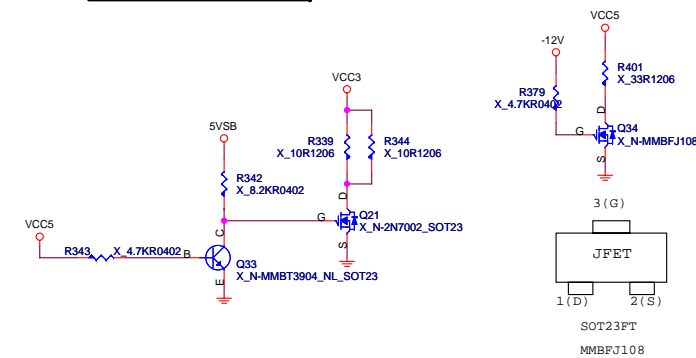
C91  
0.1u/25V/4



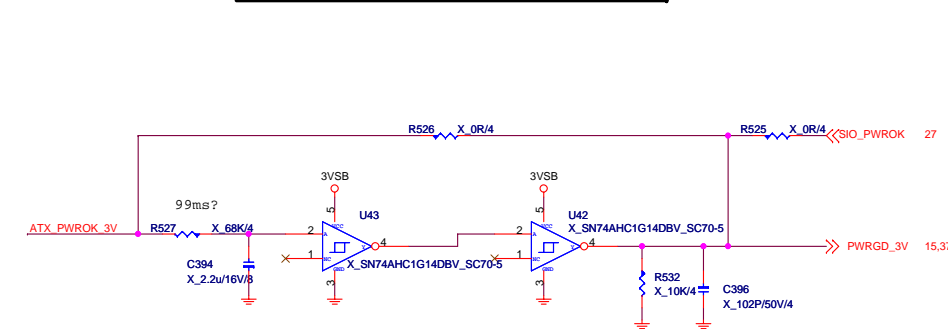
## ATX POWER CONNECTOR



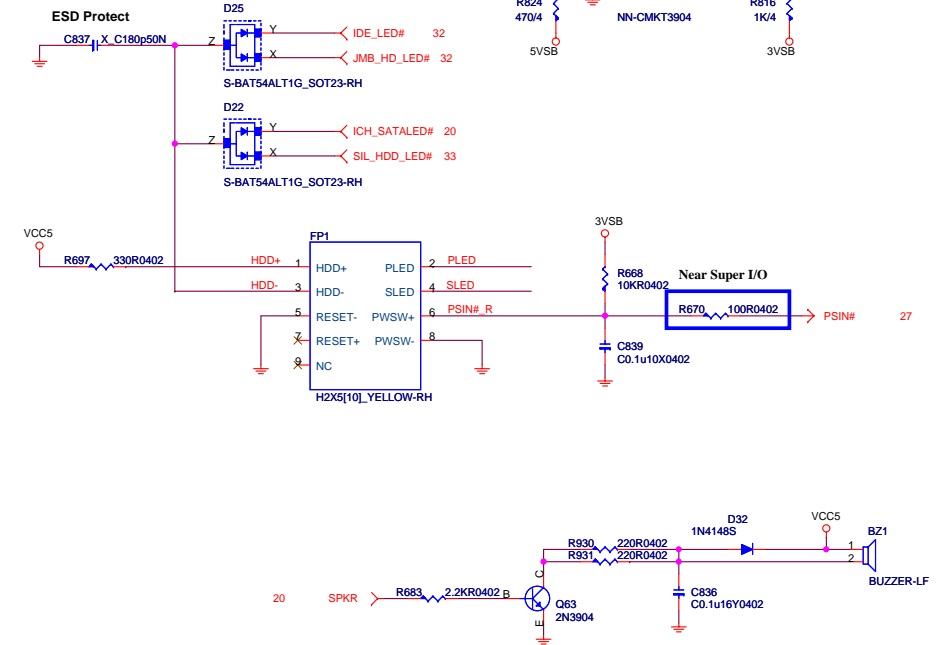
## Minimum Load



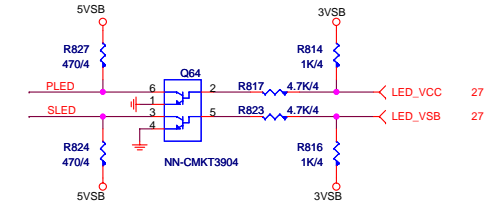
## CHIPSET POWER GOOD CIRCUIT



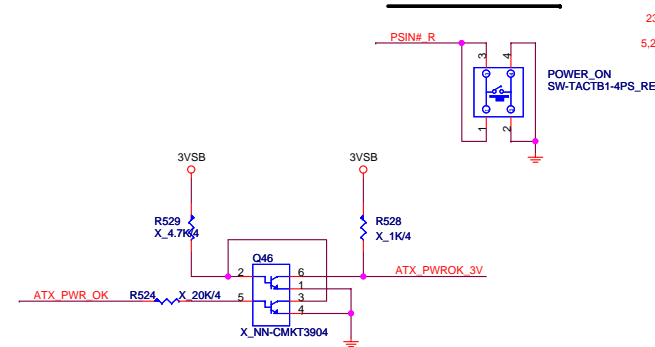
## FRONT PANNEL



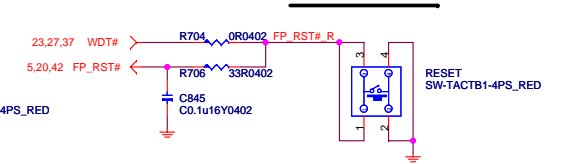
## LED ( By Fintek 71882)



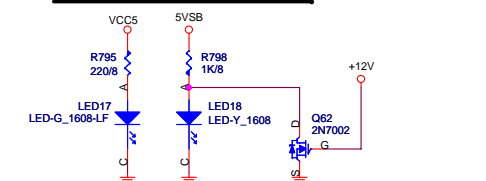
## POWER ON BUTTON



## RESET BUTTON



## POWER LED (S0/S3)





**SATA1**

Pin	Signal	Component	Pin	Signal	Component
1	GND		8	GND	
2	HT+1		9	HT+2	
3	HT-1		10	ST TX#1	C393
4	GND		11	ST TX#1	C397
5	GND		12	ST RX#1	C406
6	HR+1		13	ST RX1	C411
7	HR-1		14		
15	GND		16		

**SATA14PM\_PURPLE-RH**

**SATA2**

Pin	Signal	Component	Pin	Signal	Component
1	GND		8	GND	
2	HT+1		9	HT+2	
3	HT-1		10	ST TX#3	C470
4	GND		11	ST TX#3	C474
5	GND		12	ST RX#3	C477
6	HR+1		13	ST RX3	C479
7	HR-1		14		
15	GND		16		

**SATA14PM\_PURPLE-RH**

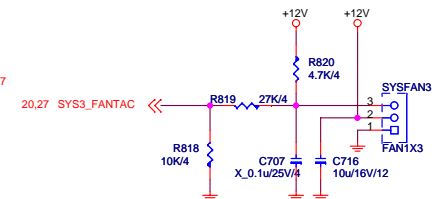
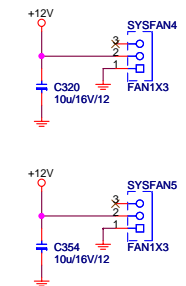
**SATA3**

Pin	Signal	Component	Pin	Signal	Component
1	GND		8	GND	
2	HT+1		9	HT+2	
3	HT-1		10	ST TX#5	C811
4	GND		11	ST TX#5	C812
5	GND		12	ST RX#5	C813
6	HR+1		13	ST RX5	C814
7	HR-1		14		
15	GND		16		

**SATA14PM\_PURPLE-RH**

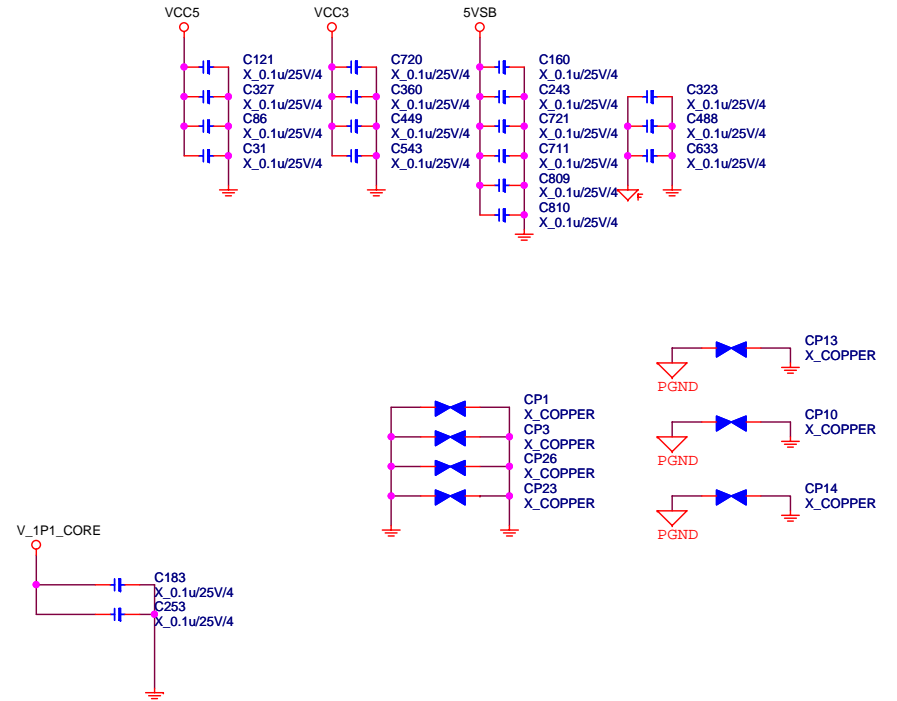
**FAN-CONTROL CIRCUIT**

The schematic diagram illustrates a fan control circuit. It features two fan drivers, SFAN1 and SFAN2, each controlled by a microcontroller (U28, W83391TG). The drivers are N-P3057LDG\_TO252-RH MOSFETs (Q58, Q47). The fans are 1N4148S diodes (D9, D11). The circuit includes various resistors (R456, R426, R414, R464, R465, R463, R567, R584, R585) and capacitors (C221, C241, C250, C466, C467, C313, C464, EC36, EC39). The fans are connected to a +12V supply and ground. The microcontroller is connected to the fans via a 12V supply and ground.



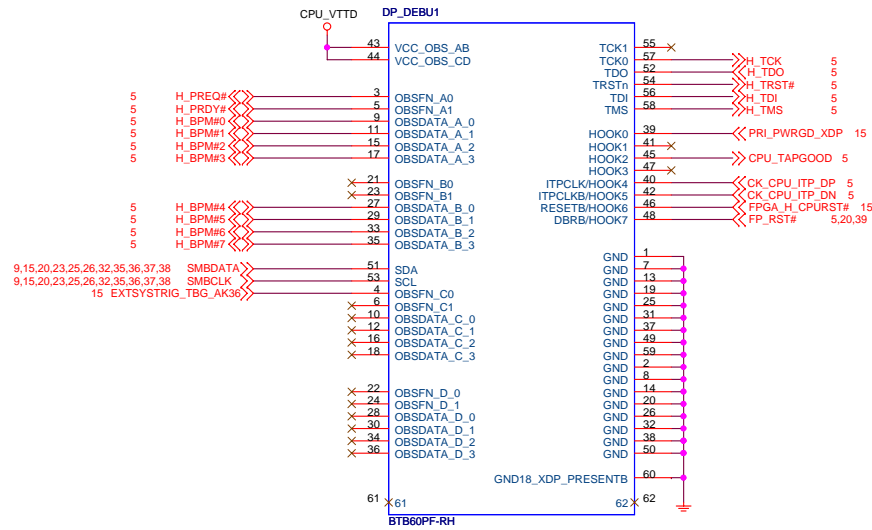


## EMI CAP

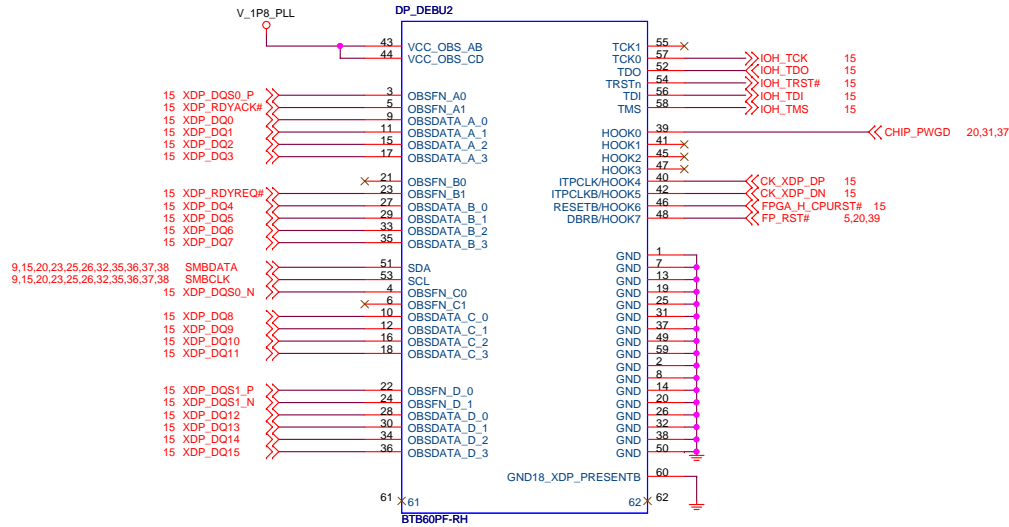




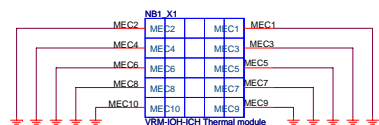
# Reserve debug port 5020



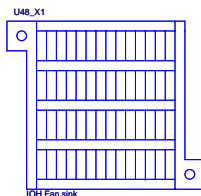
# Reserve debug port 5020







PF0-075430B-B32  
PF0-075430B-T53



BAT-BCR2032P-RH



E21-0000580

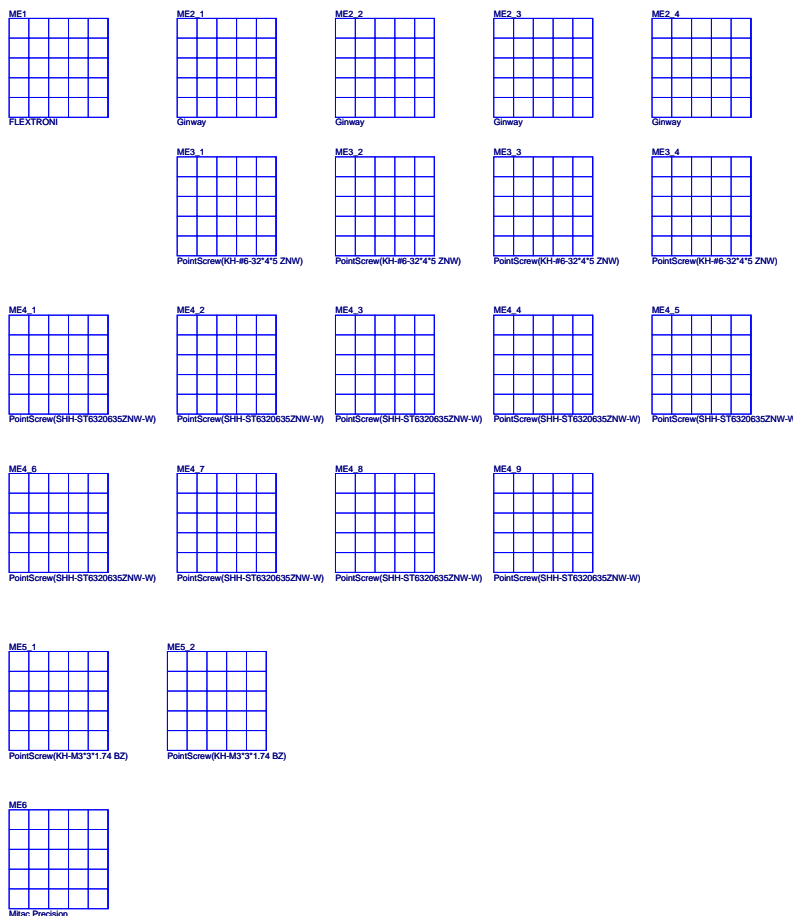
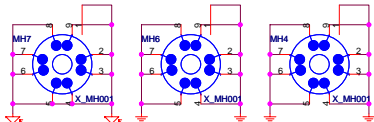
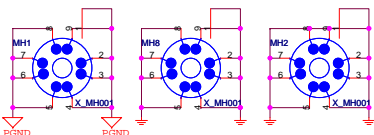
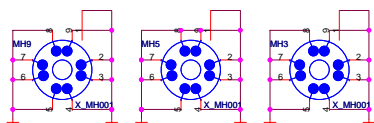
#### Optical Fiducial Marks-120



#### Optical Fiducial Marks-100



#### Mounting Holes

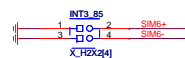


#### Simulation

4/8 95 ohm

5/5 85 ohm

5/7 85 ohm



Title		
Manual Parts		
Size	Document Number	Rev
Custom	DELL Suzuka MLK (MS-7543)	0C
Date:	Tuesday, September 09, 2008	Sheet 43 of 48